Performance and Reliability of Integrated Circuits within Computing Systems

Edward Wyrwas
DfR Solutions, LLC
5110 Roanoke Pl, Ste 101
College Park, MD 20740
ewyrwas@dfrsolutions.com

ABSTRACT
High performance computer systems, including those used for instrumentation, measurement, and advanced processing require high reliability, high quality complex integrated circuits (ICs) to ensure the accuracy of analytical data they process. Microprocessors and other complex ICs (i.e. GPGPU) are predominantly considered the important components within these systems. They are susceptible to electrical, mechanical and thermal modes of failure like other components on a printed circuit boards, but due to their complexity and roles within a circuit, performance-based failure can be considered an even larger concern. Stability of device parameters is key to guarantee a system will function according to its design. Modifications to operational parameters of these devices through over- or under-clocking can either reduce or improve overall reliability, respectively, and furthermore directly affect the lifetime of the system which it is installed in.

The ability to analyze and understand the impact that specific operating parameters have on device reliability is necessary to mitigate risk of system degradation, which will affect bus speeds, memory access, data retrieval, and even cause early failure of that system or critical components within it. An accurate mathematical approach which utilizes semiconductor formulae, industry accepted failure mechanism models, Physics-of-Failure (PoF) knowledge and more importantly, device functionality has been devised to access reliability of those integrated circuits vital to system reliability.

General Terms
Algorithms, Performance, Reliability

Keywords
Physics of Failure, PoF, Reliability, Failure Rate, Failure Mechanisms, Si, Sub-micron, Wearout

1 INTRODUCTION
Performance of computing systems can be evaluated using a number of different metrics based on the type or combination of systems; e.g. memory, file storage, databases, and networks. Developing models to analyze the performance of these systems typically includes read/write timings, memory retrieval, delay, user experience in software and the number of processing cycles to complete a task. The main similarity between these systems is that they use high performance hardware containing complex integrated circuits. These components are the underlying technology that drives system performance.

Development of these critical components has conformed to Moore's Law, where the number of transistors on a die doubles approximately every two years. This trend has been successfully followed over the last four decades through reduction in transistor sizes creating faster, smaller ICs with greatly reduced power dissipation. Although this is great news for developers of high performance equipment, a crucial, yet underlying reliability risk has emerged. Semiconductor failure mechanisms which are far worse at these minute feature sizes (tens of nanometers) result in shorter device lifetimes and unanticipated, early device wear out.

Currently, four semiconductor failure mechanisms that exist in silicon-based ICs are analyzed: Electromigration (EM), Time Dependent Dielectric Breakdown (TDDB), Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI). Mitigation of these inherent failure mechanisms, including those considered wear out failure modes, is only possible when reliability can be quantitatively calculated. Algorithms have been incorporated into a software application to not only calculate a failure rate, but also give confidence intervals and produce a lifetime curve, using both steady state and wear out failure rates, for the IC under analysis. Furthermore, the algorithms have been statistically verified through testing and employ data and formulae from semiconductor materials (to include technology node parameters), circuit fundamentals, transistor behavior, circuit design and fabrication processes. Initial development\(^1\) has yielded a user-friendly software module with the ability to address silicon-based integrated circuits of the 0.35\(\mu\)m, 0.25\(\mu\)m, 0.18\(\mu\)m, 0.13\(\mu\)m and 90nm technology nodes.

\(^1\) Development of the 0.13\(\mu\)m and 90nm technology node models was funded by Aero Engine Controls, The Boeing Company, General Electric (GE), the National Aeronautics and Space Administration (NASA), the Department of Defense (DoD), and the Federal Aviation Administration (FAA) in cooperation with the Aerospace Vehicle Systems Institute (AVSI).
1.1 Device Specifications

Individuals who entertain the idea that electronic devices with no moving parts should last forever are living in a fantasy. Those of us who work in the electronics industry know otherwise. The primary questions system designers should ask themselves are “Should devices be operated outside of their specifications?” and “Do we even know why doing this will cause damage to the device – enough damage to reduce the lifespan of our systems to inside our projected useful life?” If we had the answers to these questions, then we would already know how operating devices outside of their “typical” or “recommended” settings will affect reliability. Most components are underrated by at least 25% to increase reliability. Some components are closer to 50% derated. Integrated circuits are less tolerant to derating and uprating, but still have good margins of 5-10%. Although it would seem that derating all components would solve our reliability needs, it actually does not. One particular failure mechanism, hot carrier injection, is driven by relatively low temperatures (room temperature) compared to those of initiated by high temperature exposure.

The dominant failure mechanisms in Si-based microelectronic devices that are most commonly simulated are EM, TDDB, NBTI and HCI. Other degradation models do exist but are less prevalent. These mechanisms can be generally categorized as Steady State Failure Modes (EM and TDDB) and Wear out Failure Modes (NBTI and HCI) [9]. A brief explanation of each failure mechanism is necessary to understand their contribution to the overall device failure rate is provided later in this paper.

Failure analysis data from a telecommunications company has shown that hot carrier injection can devastate the primary computing components of a platform within a few years – even if these components were custom designed to mitigate known failure behaviors. The anticipated field life of this particular product was 15 to 20 years. Failures of this type are never anticipated, nor have they been able to be predicted in the past. Presently, it is necessary to have methods to predict the failure rate of such components, preferably easy-to-use software applications.

The idea of overclocking (uprating) should provide an almost obvious rationale that devices running above their specifications will not survive as long as a non-overclocked device. System analysis is necessary to determine how overclocking may cause system instability, i.e. timing control issues. Making a device work harder will indicatively create more heat. System designers should verify their thermal solutions are optimal for an increased system load.

Overclocking a device too much creates issues as well. Therefore, a higher degree of system analysis should be performed to see how the change in device parameters will affect it. Issues that are commonly created are noise in the signals, unforeseen reduction in threshold voltages, offset propagation delay timings, latch up and mismatched bus speeds.

Reliability of semiconductor devices may depend on assembly, use, and environmental conditions. Stress factors affecting device reliability include gas, dust, contamination, voltage, current density, temperature, humidity, mechanical stress, vibration, shock, radiation, pressure, and intensity of magnetic and electrical fields. As engineers we can design, redesign, and adjust our system to include printed circuit board type, vibration dampening and even conformal coatings or potting to reduce, or even eliminate, the effects of extrinsic failure mechanisms and stressors. However, those intrinsic to the device (sourced through its material constituents and design) are eventually going to take place. The overwhelming question is “When?”

In the electronics industry, there is an interest in assessing the long term reliability of electronics whose anticipated lifetime extends farther than consumer “throw away” electronics. Because complex integrated circuits within their designs may face wear out or even failure within the period of useful life, it is necessary to investigate the effects of use and environmental conditions on these components. The main concern is that submicron process technologies drive device wear out into the regions of useful life well before wear out was initially anticipated to occur.

2 RELIABILITY MODELING AND SIMULATION

There has been steady progress over the years in the development of a physics-of-failure understanding of the effects that various stress drivers have on semiconductor structure performance and wearout. This has resulted in better modeling and simulation capabilities. Early investigators sought correlations between the degradation of single device parameters (e.g. \( V_{th} \), \( V_{dd} \) or \( I_{on} \) ) and the degradation of parameters related to circuit performance such as the delay between read and write cycles. It was quickly realized that the degradation of a broad range of parameters describing device performance had to be considered, rather than just a single parameter [1]. Most of the simulation tools tend to simulate a single failure mechanism such as Electromigration [2],[13], TDDB [2], NBTI [9],[15] and HCI [2]. System-level simulators attempting to integrate several mechanisms into a single model have been developed as well. The latest circuit design tools, such as Cadence Ultrasim and Mentor Graphics Eldo, have integrated reliability simulators. These simulators model the most significant physical failure mechanisms and help designers address the lifetime performance requirements. However, inadequacies, such as complexity in the simulation of large-scale circuits and a lack of prediction of wearout mechanisms, hinder broader adoption of these tools [13].

2.1 Validation Concerns

Reliability simulations are commonly based on a mixture of PoF models, empirical data and statistical models developed over the years by different research groups and industries. The inevitable consequence of a wide range of models and approaches is a lack of confidence in the obtained predictions for any given model. From the point of view of a real-world end-user, single failure mechanism modeling and simulation is less meaningful then the system level reliability.

Validation and calibration of simulations is accomplished by comparing simulation predictions with empirical data obtained from lab tests or by analyzing field data. To evaluate the reliability of their devices, semiconductor manufacturers use lab tests such as environment stress screens (ESS), highly accelerated lifetime testing (HALT),
HTOL and other accelerated life tests (ALT). Several concerns shed doubt on the prediction accuracy derived from such tests. The assumption of a single failure mechanism is an inaccurate simplification of actual failure dynamics. Furthermore, ALT tests based on sampling a set of devices have the inherent problem of a lack of statistical confidence in the case of zero observed failures. Finally, ALT tests can only mimic actual field conditions to estimate real-world reliability and extrapolation from test environmental stresses to field stresses can be misleading [1, 5, 9].

2.2 Accelerated Testing to Drive Failure Mechanisms

An accelerated test is designed to speed up a behavior or mechanism that will cause the device to fail over time. Each failure mechanism has a corresponding activation energy. This activation energy is the energy necessary for a reaction or change to occur in a material. The ratios of field and test voltages and temperatures along with the activation energy can be used to calculate an acceleration factor that will correlate the lifetime under test to the expected life of the device operating in the field environment.

An integrated circuit device’s life is limited by thermal, mechanical and electrical stresses and process defects. Mechanical and process defects include wire bond issues, delamination, and thermal-mechanical mismatch between materials. Degradation mechanisms attributed to processes and environmental exposure include corrosion, mechanical overstress, stress migration, and atomic transport between lattice dislocations. The intrinsic semiconductor failure mechanisms that are modeled in this software fall into the categories of steady state and wear out. Steady state failure modes include electromigration and time dependent dielectric breakdown. The wear out failure modes include hot carrier injection and negative bias temperature instability. A definition of each of these is provided below.

Electromigration can lead to interconnect failure in an integrated circuit. It is characterized by the migration of metal atoms in a conductor in the direction of the electron flow. Electromigration causes opens or voids in some portions of the conductor and corresponding hillocks in other portions [2], [5], [13].

Time Dependent Dielectric Breakdown is caused by the formation of a conducting path through the gate oxide to the substrate due to an electron tunneling current. If the tunneling current is sufficient, it will cause permanent damage to the oxide and surrounding material. This damage will result in performance degradation and eventual failure of the device. If the tunneling current remains very low, it will increase the field necessary for the gate to turn on and impede its functionality. The gate dielectric breaks down over a long period of time for devices with larger feature sizes (>90 nm) due to a comparatively low electric field. Although core voltages have been scaled down as feature sizes have shrunk, supply voltages have remained constant. These field strengths are still a concern since high fields exacerbate the effects of TDDB [2], [5].

Hot Carrier Injection occurs in both nMOS and pMOS devices stressed with drain bias voltage. High electric fields energize the carriers (electrons or holes), which are injected into the gate oxide region. Like NBTI, the degraded gate dielectric can then more readily trap electrons or holes, causing a change in threshold voltage, which in turn results in a shift in the subthreshold leakage current. HCI is accelerated by an increase in bias voltage and is the predominate mechanism at lower stress temperatures [2], [5]. Therefore, hot carrier damage, unlike the other failure mechanisms, will not be replicated in HTOL tests, which are commonly used for accelerated life testing [1].

Negative Bias Temperature Instability occurs only in pMOS devices stressed with a negative gate bias voltage while at elevated temperatures. Degradation occurs in the gate oxide region allowing electrons and holes to become trapped. Negative bias is driven by smaller electric fields than hot carrier injection, which makes it a more significant threat at smaller technology nodes where increased electric fields are used in conjunction with smaller gate lengths. The interface trap density generated by NBTI is found to be more pronounced with thinner oxides [5], [9], [15].

2.3 An Accelerated Test’s Failure Rate

The beginning phases of analysis should include a brief summary of mechanisms and their activation energies the will cover factors that affect semiconductor lifetimes relevant to the device under analysis. An explanation of mechanisms and their activation energies will determine which one(s) should be used in Arrhenius relationship (temperature dependent reactions) based accelerated life testing. In real world environments, multiple failure mechanisms will be activated which will have various levels of impact on the device lifetime. Therefore, it is not representative to say that testing to one failure mechanism’s activation energy will induce all types of failures.

Industry uses a standard test for semiconductor devices. However, these tests do not take into account the materials, technology, complexity or function of the device. JEDEC Standard number 47D, “Stress-Test-Driven Qualification of Integrated Circuits,” defines this typical acceleration test style which is a high temperature operating life test. The test is based on three (3) lots of 77 parts per lot. The test duration is 1000 hours with a test temperature of +125°C. The total duration of the test upon completion is 231,000 hours from:

\[ T_{test} = 3 \text{ lots x 77 samples x 1000 hours} = 231,000 \text{ device hours} \]

When we talk about uprating or derating a device, we are considering applying an acceleration factor to its anticipated life. Acceleration factors are the extrapolation between test and field conditions at one set of given points. Traditionally, only voltages and temperatures are accelerated.

The acceleration factor due to changes in temperature is the acceleration factor most often referenced (JEDEC Publication No. 122B). The mathematical relationship follows the format of the Arrhenius equation:

\[ AF = \frac{\lambda_{test}}{\lambda_{field}} = EXP \left( \left( \frac{-Ea}{K} \right) \left( \frac{1}{T_{test}} - \frac{1}{T_{field}} \right) \right) \]

Where:

- \( Ea \) is the activation energy in electron volts (eV);
- \( K \) is Boltzmann's constant (8.62x10^-5 eV/K);
$T_{\text{Test}}$ is the absolute temperature of the test (K); $T_{\text{Field}}$ is the absolute temperature of the system (K); $\lambda_{\text{Test}}$ is the failure rate at the test temperature; $\lambda_{\text{Field}}$ is the failure rate at the actual field temperature.

Thus, when predicting failure rate from HTOL test results, $E_a$ and $T_{\text{Field}}$ are considered indispensable.

Activation energy is the parameter used to express the degree of acceleration related to temperature. Single failure mechanisms are accompanied by unique activation energy values (JEDEC Publication No. 122B). However, it is a traditional method to use an activation energy of 0.7eV as it is generally assumed as average activation energy during the useful life of a device. This useful life lies beyond the early stages of infant mortality failures (manufacturing defect driven failures). Industry is widely using this value of 0.7eV in the following two cases:

1. When estimating an overall failure rate without focusing in a single failure mechanism. It is assumed to be a conservative value with regarding the mixture of single mechanisms activation energies.
2. When the failure mechanisms degrading a device are unknown.

The industry aim in using HTOL is to gain maximum possible acceleration to accumulate maximum equivalent field time, with zero failures. (Yes, zero failures. Some device manufacturers will retest until they achieve zero failures. The user will never see the testing results, nor will they know that failures did occur during another test.) Assuming higher activation energies will serve this target, on one hand, but reduce the failure rate upper limit, on the other hand. For example, assuming activation energy of 1.0eV instead of 0.7eV will raise the acceleration factor to 504 instead of 78 (6.5 times more). On the other hand, the failure rate will reduce from 51 FIT to level of only 8 FIT, which is even more optimistic.

If we were to design a test around an activation energy, we could make that test longer or shorter than 1000 hours. Either way, we would be modifying the testing conditions for our gain, in the eyes of management, not for an understanding of a device's ACTUAL reliability. A new approach at calculating failure rates for semiconductor devices would be beneficial to industry.

3 INTEGRATED CIRCUIT LIFETIME

The goal is to determine how uprating or derating system parameters (or just changing the field environment) will affect an integrated circuit. This is typically called trade-off analysis. If we have our inputs set up with an equation and can plot our results in a spreadsheet, then we should be able to tweak the inputs and see how the outputs are affected. This sounds like a simple concept; and it is.

Let us re-emphasize this point: The temptation will be to blame device failure on how it was operated. A better approach, however, is to consider manufacturing methods and technology inside the device since it has no moving parts.

DfR Solutions, LLC, has developed an integrated circuit (IC) reliability calculator using a multiple failure mechanism approach. This approach successfully models the simultaneous degradation behaviors of multiple failure mechanisms on integrated circuit devices. The multiple mechanism model extrapolates independent acceleration factors for each semiconductor mechanism of concern based on the transistor stress states within each distinct functional group. Integrated circuit lifetime is calculated from semiconductor materials and technology node, IC complexity, and operating conditions.

Smaller and faster circuits cause higher current densities, lower voltage tolerances and higher electric fields, which make integrated circuits more vulnerable. New generations of electronic devices and circuits demand new means of investigation to check the possibility of introducing either new problems or new versions of old issues. The arrival of new devices with new designs and materials require failure analysis to find new models for both the individual failure mechanisms and also the possible interactions between them. The interaction of multiple failure mechanisms is one of the issues that requires serious investigation.

In the sub-micrometer region, reliability has been overlooked in favor of performance. Proper tradeoffs in the early design stage are a dominating challenge. After performing a quick and effective reliability analysis, both lifetime estimation for the device and failure mechanism dominance hierarchy are achieved. Using reliability knowledge and improvement techniques, higher reliability integrated circuits can be developed using two methods: suppress die-level failure mechanisms and adjust circuit structures. This has been realized for electromigration (through Black's equation [5]) using design techniques, however, it is counter-productive across industry in the aims of device scaling to adjust transistor sizes. Redesign of transistor architecture and circuit schematics is too resource intensive both in time and cost to be the corrective action for reliability concerns. The end user must decide what reliability goals need to be achieved; more so, it has become his responsibility to determine how to achieve those goals without any influence on component design, manufacturing, or quality. This type of reliability assessment is crucial for the end user as adjustments to electrical conditions and thermal management seem to be the only way to improve reliability of modern technology nodes. The tradeoff in performance can be significantly reduced by using devices from larger technology nodes as they provide larger operating tolerances and the architectures necessary to reduce the effects of multiple mechanism degradation behaviors.

As technology shifts to the smaller nodes, the operating voltage of the device is not reducing proportionally with the gate oxide thickness, which results in a higher electric field; moreover, the increasingly denser number of transistors on a chip causes more power dissipation and in turn an increased operating temperature through self-heating. Conversely, introducing nitrogen into the dielectric to aid in gate leakage reduction together with boron penetration control has its own effect - linearly worsening NBTI and other modes of degradation. Because the threshold voltage of new devices is
not being reduced proportional to the operating voltage, there would be more degradation for the same threshold voltage.

3.1 PRACTICAL IMPLEMENTATION OF A PREDICTION METHOD

Preliminary analysis of the device uses a process that categorizes an integrated circuit into smaller functional blocks to apply acceleration factors at the most minute level. Equivalent function sub-circuits are used as part of the calculator to organize the complexity of the integrated circuit being analyzed into functional group cells, i.e. one (1) bit of DRAM. The functional group block diagram for National Semiconductor's 12-bit ADC component, ADC124S021, is shown in Figure 1. It contains a multiplexer group, track and hold function, control logic, and 12-bit analog-to-digital converter.

The software has the ability to take two approaches to analyze the failure mechanism contributions to the failure rate of each device. These are Independent of Transistor Behavior (ITB) and Dependent on Transistor Behavior (DTB). It makes two assumptions that are shown in research documents from NASA/JPL and the University of Maryland where the Multiple Mechanism approach was initially researched:

1. In an integrated circuit, each failure mechanism has an equal opportunity to initiate a failure, and
2. each can take place at a random interval during the time of operation

In ITB, the weight factors of the failure mechanisms are spread out evenly over transistor types within each functional group. Only three mechanisms affect nMOS transistors, EM, HCI, and TDDB, therefore each have 33% contribution. All four mechanisms affect pMOS transistors, therefore each have a 25% contribution. These weight factors are the same for each functional group type as well. The DTB process utilizes back-end SPICE simulation to determine the failure mechanism weighting contributions based on transistor behavior and circuit function. Using these mechanism weighting factors, sub-circuit cell counts, and transistor quantities, an overall component failure rate is calculated.

The overall software assumes that all the parameters for these models are technology node dependent. It is assumed that the technology qualification (process qualification) has been performed and at least one screening has occurred before a device is packaged. This reliability prediction covers the steady-state random failures and wear out portions of the bathtub curve.

The standard procedure for integrated circuit analysis uses high temperature operating life (HTOL) test conditions for the test conditions used for extrapolation. These parameters include ambient temperature of the test environment and the supply and core voltages of the integrated circuit. The HTOL ambient temperature was calculated for each component (except when supplied by the manufacturer). Thermal information was gathered from the datasheet and/or thermal characteristic documentation and each manufacturer's website. Using Equation 1, junction temperature, power dissipation, and junction-to-air thermal resistance are used to calculate ambient temperature.

$$T_A = T_J - P_D * \Theta_{J-A}$$

Equ 1

Junction-to-air thermal resistance was found either on a component's datasheet or in thermal characteristic databases for package type and size; i.e. Texas Instruments or NXP Semiconductors websites. The ambient temperature calculation for a sample component is shown in Equation 2.

$$T_A = 85^\circ C - (0.446W * 51^\circ C/W)$$

$$T_A = 62.25^\circ C$$

Equ 2

Inputs on the calculator are the test parameters and results from the standard JEDEC accelerated test and information pertaining to the integrated circuit:

- **JEDEC Standard No. 47D**
  - 25 devices under test
  - 1000 hour test duration
  - zero (0) failures
  - 50% confidence level

- Pre- or user-defined process node parameters

- Device complexity as broken down by functional groups and quantity of cells within each functional group, where applicable

- Accelerated test information (qty. of failures, qty. of devices, test duration)

- Duty cycle of device (i.e. diurnal cycling or 50%)

- Confidence level of calculation/test

- Field and test conditions (field conditions allow for multiple operating modes)
  - ambient temperature
  - operating frequency

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2 Joint Electronic Devices Engineering Council, JESD 47D: Stress-Test Driven Qualification of Integrated Circuits
4 SYSTEM RELIABILITY MODELING

Our approach is to model useful life failure rate (FIT) for components in electronic assemblies by assuming each component is composed of multiple sub-components, for example: a certain percentage is effectively ring-oscillator, static SRAM, DRAM, etc. Each type of circuit, based on its operation, can be seen to affect the potential steady-state (defect related) failure mechanisms differently based on the accelerated environment, for example: Electromigration, Hot-Carrier, NBTI, etc. Each mechanism is known to have its own acceleration factors with voltage, temperature, frequency, cycles, etc. Each sub-component will be modeled to approximate the relative likelihood of each mechanism per sub-component. Then, each component can be seen as a matrix of sub-components, each with its own relative weight for each possible mechanism.

4.1 Mathematical Theory

Each failure mechanism described above would have a failure rate, $\lambda$, driven by a combination of temperature, voltage, current, and frequency. Parametric degradation of each type affects the on-die circuitry in its own unique way; therefore, the relative acceleration of each one must be defined and averaged under the applied condition. The failure rate contribution of each can be normalized by taking into account the effect of the weighted percentage of that failure rate. We ignore interactions between failure mechanisms for practical reasons although deeper studies of potential interactions could be made in the future. For the four mechanisms of EM, HCI, NBTI and TDDB, the normalized failure rate can be defined as $\lambda_{EM}$, $\lambda_{HCI}$, $\lambda_{NBTI}$ and $\lambda_{TDDB}$ respectively. In order to achieve more accuracy in the overall failure rate estimation, it is useful to split the IC into equivalent function sub-circuits and refer to it as a system of functional group cells, for example: 1 bit of SRAM, 1 bit of DRAM, one stage of a ring oscillator, and select modules within Analog-to-Digital circuitry (ADC), etc. For each functional group type, the failure rate can be defined as a weighted summation of each failure rate type multiplied by a normalization constant for the specific failure mechanism.

$$\lambda_F^1 = \sum (K_{i,F} \times \lambda_i)$$

Equ 3

Where $\lambda_F^1$ is the failure rate of one unit of functional group, $F$. $K_{i,F}$ is a constant defined by the weight percentage of functional group $F$ as it affects the $i^{th}$ failure mechanism and $\lambda_i$ is the normalized failure rate of any failure mechanism. For example, the failure rate of electromigration affecting a DRAM group would be:

$$K_{EM,DRAM} \times \lambda_{EM}$$

where $K_{EM,DRAM}$ is a constant defining the weight percentage that DRAM has on the normalized electromigration failure rate. The overall DRAM failure rate per functional group, $\lambda_{DRAM}^1$, is:

$$\lambda_{DRAM}^1 = K_{EM,DRAM} \times \lambda_{EM} + K_{HCI,DRAM} \times \lambda_{HCI} + K_{NBTI,DRAM} \times \lambda_{NBTI} + K_{TDDB,DRAM} \times \lambda_{TDDB}$$

Equ 4

Where $K_{EM,DRAM}$ is a constant defined by the weight percentage that DRAM has on Electromigration, $\lambda_{EM}$ is the normalized failure rate of Electromigration, $K_{HCI,DRAM}$ is a constant defined by the weight percentage that DRAM has on HCI, $\lambda_{HCI}$ is the normalized failure rate of HCI, $K_{NBTI,DRAM}$ is a constant defined by the weight percentage that DRAM has on NBTI, $\lambda_{NBTI}$ is the normalized failure rate of NBTI, $K_{TDDB,DRAM}$ is a constant defined by the weight percentage that DRAM has on TDDB and $\lambda_{TDDB}$ is the normalized failure rate of TDDB.

Considering the probability of a specific functional group being operationally active at the instance when failure occurs is a modification to Equation Equ 3:

$$\lambda_F = P_F \times \lambda_F^1 = P_F \times \sum (K_{i,F} \times \lambda_i)$$

Equ 5

Where $\lambda_F$ is the failure rate of a functional group as the cause of the potential failure of the device under analysis and $P_F$ is the probability that that functional group was operational during failure. The total failure rate of a component, $\lambda_T$, can be defined as being equal to the summation of the total number of each functional group multiplied by the failure rate of each functional group type

$$\lambda_T = \sum N_F \lambda_F = N \times \sum (N_F/N) \times \lambda_F = N \times \sum A_F \times \lambda_F$$

Equ 6

Where $\lambda_T$ is the failure rate of the component under analysis, $N_F$ is the total number of each function group, $N$ is the total number of all types of function groups and $A_F$ is the ratio of the number of units of the $n$th functional group type to the total number of functional groups that exist in the component under analysis. The prediction process is demonstrated in Figure 2.
4.2 Validation

DfR Solutions performed an extensive validation study in cooperation with a telecommunications company. Actual field data were extracted from a database, which encompasses shipments and customers’ claims. Unique identifiers of each product and failure enabled the detailed statistical field analysis. The ICs were assembled on boards belonging to a family of communication products shipped during 2002-2009. Component complexity and electrical characteristics were extracted from corresponding component documentation for use in the calculator. The reliability calculations are based on the time domain of the host computer. Except for the microcontroller, which is stressed 24 hours a day, we assume that memory parts and the processor are partly stressed depending on the user profile. A conservative assumption is that a regular user will stress the parts two shifts/day, i.e. 16 hours/day.

A statistical analysis comprised of Weibull and exponential analysis was used to calculate a field failure rate of five (5) integrated circuits that were identified as the root cause of failure in their respected assemblies. In a parallel activity, each of these components was "soft" analyzed by simply reading datasheet and thermal/package documentation. Using the methodology described in this article to acquire the inputs to the IC lifetime calculator, failure rates for each integrated circuit were calculated. Table 1 shows the field, predicted and the traditional HTOL failure rates for each component.

<table>
<thead>
<tr>
<th>Component</th>
<th>Field</th>
<th>Predicted</th>
<th>HTOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>256MB DRAM</td>
<td>689</td>
<td>730</td>
<td>51</td>
</tr>
<tr>
<td>512MB DRAM</td>
<td>415</td>
<td>418</td>
<td>51</td>
</tr>
<tr>
<td>1GB DRAM</td>
<td>821</td>
<td>1012</td>
<td>51</td>
</tr>
<tr>
<td>Microcontroller</td>
<td>220</td>
<td>249</td>
<td>51</td>
</tr>
<tr>
<td>Pentium Processor</td>
<td>144</td>
<td>291</td>
<td>51</td>
</tr>
</tbody>
</table>

It should be noted that the DRAM failure rates presented in Table 1 and Figure 3 refer to critical faults, which forced the user to replace the part. They do not reflect specific rates of different types of errors (correctable or non-correctable, i.e. single event upset caused by radiation) but rather a complete part failure rate.

As you can see from the results, it is possible to accurately predict the failure rate of an integrated circuit. This answers our "when might failure occur" question. Now, having a realistic data point to start with, trade-off analysis can ensue and we can see how uprating or derating devices will affect their reliability and performance.

Several commercial organizations have indicated a willingness to assist with the development and validation of 45nm technology through IC test components and acquisition of field failure data. Testing individual transistors and their stress states should provide the individual building points and data necessary to expand into any circuit function. Continued development would incorporate this information, additional material sets such as silicon on insulator, and expand into functional groups relevant for analog and processor based (e.g. DSP and FPGA) integrated circuits. Our capabilities currently include major technology nodes of the CMOS process on the International Technology Roadmap for Semiconductors (ITRS) from 0.35 micron through 90nm.
5 REFERENCES

1. Aerospace Vehicle Systems Institute (AVSI) project AFE 17 reports