Network-processing hardware specifications: an overview of the LA-1 specification

The LA-1 specification is the look-aside interface to the network-processing element (NPE). Read on to find out more.

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The work on the LA-1 specification, the look-aside interface to network-processing elements (NPEs), started at the beginning of 2001 and became an approved Network Processing Forum (NPF) specification in May 2002. Work on the LA-1 specification was done in the Look Aside Task Group, Hardware Working Group of the NPF, whose charter is defining and delivering hardware interfaces for the components located adjacent to an NPE via the look-aside interface.

Figure 1 depicts the system block diagram and highlights the look-aside interface. This interface targets devices that off load certain tasks from the NPE.

![Figure 1: System block diagram](image)

The LA-1 interface primarily targets (though not exclusively) look-up- and memory-based coprocessors and emphasizes as much as possible the use of existing technology. It is based on QDR and SigmaRAM technologies. The LA-1 interface operates at speeds of 133 to 200 MHz. Although modeled on an SRAM interface, the LA-1 specification aims to accommodate other device types; it targets devices such as ternary content-addressable memories (TCAMs), classifiers, and encryption coprocessors.

The LA-1 interface aims to support the transaction requirements for OC-48 through OC-192 line rates. The performance specification for coprocessors is four transactions at OC-48 or one transaction at OC-192. Packet-count assumptions are for line-rate performance using 40-byte packets and 144-bit transactions.

The LA-1 interface features include:

- Concurrent read and write operation
- Unidirectional read and write interfaces
• Single address bus
• An 18-pin DDR data-output path that transfers 32 bits plus 4 bits of even-byte parity per read
• An 18-pin DDR data-input path that transfers 32 bits plus 4 bits of even-byte parity per write

The LA-1 data inputs and outputs are separate and operate simultaneously, thus eliminating the need for high-speed bus turnaround. The LA-1 specification defines signals for host and slave devices. It defines an input master clock, a data clock, and an echo clock. The input master clock is mandatory for both slave and host devices. The data clock is optional for host devices and mandatory for slave devices. The echo clock is optional for slave devices and mandatory for host devices.

The specification allows three possible implementations for the data-output control on slave devices. A slave device may or may not provide echo-clock outputs. If it does not implement such outputs, assume that output data is controlled by and referenced to the data clock. If the data clock is absent, the output data is controlled by and referenced to the input master clock.

The LA-1 interface can sustain both a read and a write operation on each clock cycle. You achieve access to the read and write ports using the same address bus.

LA-1 also provides an option for depth expansion while the chip enables input. Programmability of two enable inputs would allow four banks of depth expansion to be accomplished with no additional logic.
LA-1 interface architecture

Figure 2 depicts a diagram showing the LA-1 interface major signals.

![Diagram of LA-1 interface major signals](image)

**Figure 2: LA-1 interface major signals**

The LA-1 interface transfers information between a Network Processing Element (Host) and a Co-Processor/Memory (Slave). Figure 2 shows the major signals involved in this interface:

- Mater Clocks
- Data Clocks
- Address
- Data Input
- Parity Input
- Data Output
- Parity Output
- Echo Clocks
- Read Select
- Write Select

The LA-1 interface transfers information between an NPE and memory or coprocessor. One LA-1 port includes a clock, address and control pins, 16 data and two parity pins for write operations, and 16 data and two parity pins for reads.

The LA-1 interface requires a master-clock pair. The master clocks are ideally 180 degrees out of phase with each other, and they are outputs for the host device, the NPE, and inputs for the slave device. The NPE must have a data-clock-pair output, and the coprocessors can optionally have a data-clock-pair input. The data clocks are ideally 180 degrees out of phase with each other and provide a way to control device-output data.

LA-1 interface ports follow a few simple rules:

- Control inputs are always captured on the rising edge of the master clock.
- Address and data are captured on the rising edges of the master clock and master-clock bar.
- Read or write data transfers in progress may not be interrupted and restarted.

The LA-1 interface provides a separate I/O-bus structure that is optimal for balanced read/write bandwidth. Even though TCAM searches can require more write bandwidth, having separate
I/Os for reads and writes is a good compromise because it is easier to design systems at high speed.

Separate I/O LA-1 ports offer two mechanisms for controlling the output-data registers. At the coprocessor, control is typically handled by the data-clock input. The data-clock input can be used to make small phase adjustments in the driving of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the master clock and master-clock bar.

**Write and read operations**

Asserting the write-select input low at the master-clock rising edge initiates a write cycle. The following master-clock-bar rising edge provides the address for the write cycle. At the same cycle, you can expect data at the rising edge of the master clock and master clock bar (**Figure 3, below**).

Each loaded write command and write address provides the base address for a “2-beat” data transfer, so 32 data bits plus four even-byte parity bits are transferred for each address loaded. By using the byte-write control signals, any byte may be masked in any write sequence.

Asserting the read-select input low at the master-clock rising edge initiates a read cycle, and the address bus presents the read address. Data is delivered after the next rising edge of the master clock, using the data clocks as the output timing references (**Figure 3, below**).

In the case of an SRAM, a read can immediately follow a write even if they are to the same address. In the case of a coprocessor, a minimum latency that is dependent on the architecture of the coprocessor will exist between a write and a read to the same address.
LA-1 logical layer

The LA-1 interface uses an SRAM-style memory-mapped structure. The interface uses an address bus to provide the network-processing unit (NPU) with the ability to control coprocessor functions. As needed, address pins address logical registers on the device. The NPU uses register-style read and write operations to initiate coprocessor actions, retrieve results, and optionally provide in-band management. A memory-mapped logical layer provides a flexible interface for coprocessor applications. Therefore, coprocessor architectures may provide differentiation and innovation because the logical layer does not excessively limit the designer.

I/O technology

I/O technology is the standardized JEDEC HSTL. LA-1 has an HSTL input-reference voltage, VREF, which provides a reference voltage for the HSTL input-buffer trip point.

Depth expansion

Devices compliant with the LA-1 specification may implement chip-enable inputs. Programmability of two enable inputs allows you to achieve four banks of depth expansion with no additional logic. By programming the enable inputs of four LA-1 ports in binary sequence...
(00, 01, 10, 11) and driving the enable inputs with two address outputs, four LA-1 ports can seem like one port with a larger address space to the system.

**Figure 4** depicts one example of the LA-1 interface in use for depth expansion.

**Figure 4: Depth-expansion example**

**Echo clocks**

The NPE must have echo-clock and echo-clock-bar inputs, and the coprocessor can optionally have echo-clock and echo-clock-bar outputs. If you use the echo clocks in a system, they track the performance of the output drivers. They are delayed copies of the data clocks. They aim to track changes in output-driver delays due to variance in die temperature and supply voltage. The echo clocks also aim to drive simultaneously with the data-output drivers.

The LA-1 specification provides for three possible implementations for the data-output control on slave devices. A slave device may or may not provide echo-clock outputs. However, if the slave device implements echo clocks, data-valid times are referenced to echo-clock edges, and the LA-1 specification describes the specifications.

A slave device that implements echo clocks may or may not choose to implement a DLL to lock the echo clocks to the data clocks.
Slave devices without echo clocks

If the slave device does not implement echo-clock outputs, assume that output data is controlled by and referenced to the data clock. Figure 5 shows the timing diagram for a slave device without echo clocks.

Slave devices without DLL-based echo clocks

If the slave device implements echo-clock outputs and the echo clocks are not locked to the input clocks, assume that output data is controlled by and referenced to the echo clocks. Figure 5 shows the timing diagram for a slave device that implements echo clocks without locking them to the input clocks.

![Figure 5: Timing diagram for a slave device using the echo clocks without DLL](image)

Slave devices with DLL-based echo clocks

If the slave device implements a DLL to lock the echo clocks to either the master clocks or the data clocks, the output data tightly couples to the input clocks. This scenario incurs an extra ½ clock cycle of input clock to data-output latency (Figure 6). In this case, assume that output data is controlled by and referenced to the echo clocks.
For more information
Full details on the LA-1 specification, specification number NPF-LA1-01.0, are available from the NPF, www.npforum.org/ApprovedSpecs.htm.

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