CHAPTER 1
Overview of Power Factor Correction Approaches

ABSTRACT

Designing power factor correction (PFC) into modern switched-mode power supplies (SMPS) has evolved over the past few years due to the introduction of many new controller integrated circuits (ICs). Today, it is possible to design a variety of PFC circuits with different modes of operation, each with its own set of challenges. As the number of choices has increased, so has the complexity of making the choice and then executing the design. In this chapter, the design considerations and details of operation for the most popular approaches are provided.

Introduction

Power factor correction shapes the input current of off-line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that emulates a pure resistor, in which case the reactive power drawn by the device is zero. Inherent in this scenario is the absence of input current harmonics—the current is a perfect replica of the input voltage (usually a sine wave) and is exactly in phase with it. In this case the current drawn from the mains is at a minimum for the real power required to perform the needed work, and this minimizes losses and costs associated not only with the distribution of the power, but also with the generation of the power and the capital equipment involved in the process. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

Another reason to employ PFC in many of today’s power supplies is to comply with regulatory requirements. Today, electrical equipment in Europe and Japan must comply with the IEC61000-3-2. This requirement applies to most electrical appliances with input power of 75 W (Class D equipment) or greater, and it specifies the maximum amplitude of line-frequency harmonics up to and including the 39th harmonic. Additionally, many energy efficiency requirements also carry a PFC requirement such as the Energy Star 5.0 for Computers and Energy Star 2.0 for External Power Supplies, and for TV effective November 2008.

Definition

Power factor correction is simply defined as the ratio of real power to apparent power, or:

\[
PF = \frac{\text{Real Power}}{\text{Apparent Power}} \quad \text{(expressed in Watts)}
\]

\[
\text{Apparent Power} \quad \text{(expressed in VA)}
\]

where the real power is the average, over a cycle, of the instantaneous product of current and voltage, and the apparent power is the product of the rms value of current times the rms value of voltage. If both current and voltage are sinusoidal and in phase, the power factor is 1.0. If both are sinusoidal but not in phase, the power factor is the cosine of the phase angle. In elementary courses in electricity this is sometimes taught as the definition of power factor, but it applies only in the special case, where both the current and voltage are pure sine waves. This occurs when the load is composed of resistive, capacitive and inductive elements and all are linear (invariant with current and voltage).

Switched-mode power supplies present nonlinear impedance to the mains, as a result of the input circuitry. The input circuit usually consists of a half-wave or full-wave rectifier followed by a storage capacitor capable of maintaining a voltage of approximately the peak voltage of the input sine wave until the next peak comes along to recharge the capacitor. In this case current is drawn from the input only at the peaks of the input waveform, and this pulse of current must contain enough energy to sustain the load until the next peak. It does this by dumping a large charge into the capacitor during a short time, after which the capacitor slowly discharges the energy into the load until the cycle repeats. It is not unusual for the current pulse to be 10% to 20% of the cycle, meaning that the current during the pulse must be 5 to 10 times the average current. Figure 1–1 illustrates this situation.
Note that the current and voltage are perfectly in phase, in spite of the severe distortion of the current waveform. Applying the “cosine of the phase angle” definition would lead to the erroneous conclusion that this power supply has a power factor of 1.0.

Figure 1–2 shows the harmonic content of the current waveform in Figure 1–1. The fundamental (in this case 60 Hz) is shown with reference amplitude of 100%, and the higher harmonics are then given with their amplitudes shown as percentages of the fundamental amplitude. Note that the even harmonics are barely visible; this is a result of the symmetry of the waveform.

Since only the fundamental component produces real power, while the other harmonics contribute to the apparent power, the actual power factor is well below 1.0. This deviation is represented by a term called distortion factor and is primarily responsible for the non-unity power factor in SMPS. The general equation governing the relationship between the real power and apparent power is given by:

\[
\text{Real power expressed in W} = \frac{\text{Apparent power expressed in VA}}{\cos \phi \cdot \cos \theta}
\]

Where \(\cos \phi\) is the displacement factor coming from the phase angle \(\phi\) between the voltage and current waveforms and \(\cos \theta\) is the distortion factor. Incidentally, the power factor of the power supply with the waveform in Figure 1–2 is approximately 0.6.
For reference, Figure 1–3 shows the input of a power supply with perfect power factor correction. It has a current waveform that mimics the voltage waveform, both in shape and in phase. Note that its input current harmonics are nearly zero.

![Figure 1–3. Input Characteristics of a Power Supply with Near–Perfect PFC](image)

**Power Factor Correction vs. Harmonic Reduction**

It is clear from the previous illustrations that high power factor and low harmonics go hand-in-hand. It is generally thought that specifying limits for each of the harmonics will do the better job of controlling the “pollution” of the input current, both from the standpoint of minimizing the current and reducing interference with other equipment. So, while the process of shaping this input current is commonly called “power factor correction,” the measure of its success in the case of the international regulations is the harmonic content. In the case of SMPS, usually the displacement factor is close to unity, so the following relationships between the harmonic distortion and power factor apply.

\[
\text{THD(\%)} = 100 \cdot \sqrt{\sum_{n=2}^{\infty} \frac{|I_n|^2}{|I_1|^2}} \quad \cos \theta = \text{PF} = \sqrt{\frac{1}{1 + \text{THD}^2}}
\]

Here, THD is the Total Harmonic Distortion which is quadratic sum of the unwanted harmonics over the fundamental that gives the relative weight of the harmonic content with respect to the fundamental. The second equation uses the absolute value of THD (not percentage) and demonstrates that THD has to be zero for PF to be unity.

**Types of Power Factor Correction**

The input characteristics shown in Figure 1–3 were obtained with “active” power factor correction, using a switched-mode boost converter placed between the input rectifier and the storage capacitor, with the converter controlled by a PFC IC (Integrated Circuit) and its attendant circuitry in a manner to shape the input current to match the input voltage waveform. This is the most popular type of PFC used in today’s power supplies, as shown in Figure 1–4. It isn’t the only type, however. There are no rules demanding that the PFC task be accomplished by active circuits (transistors, ICs, etc.). Any method of maintaining the harmonics below the regulatory limits is fair game. It turns out that one inductor, placed in the same location as the active circuit, can do the job. An adequate inductor will reduce the peaks of the current and spread the current out in time well enough to reduce the harmonics enough to meet the regulations. This method has been used in some power supplies where the large size of the inductor and its weight (due to its iron core and copper winding) are not objectionable. At higher power levels, the size and weight of the passive approach become unpopular. Figure 1–5 shows the input characteristics of three different 250-W PC power supplies, all with the current waveforms at the same scale factor. As shown, the peak current levels in passive PFC circuit are still 33% higher than the peak currents in active circuits. In addition, while the harmonic levels of the second levels may meet the IEC61000-3-2, it will fail the more stringent 0.9 PF requirement being imposed by some recent regulations.
In recent years, market trends (rising cost of copper and magnetic core material and falling costs of semiconductors) have tilted the balance decidedly in favor of active PFC even in the most cost-sensitive consumer applications. Coupled with the additional system benefits afforded by the active PFC circuits [1], this seems to be a trend that is likely to continue in the future and lead to more advanced active PFC solutions becoming available to the designers.

**Figure 1–4. PFC Preconverter Stage**

**Figure 1–5. Input Characteristics of PC Power Supplies with Different PFC Types (None, Passive, and Active)**

**Input Line Harmonics Compared to IEC61000-3-2**

Figure 1–6 shows the input harmonics of three 250-W PC power supplies, along with the limits according to IEC61000-3-2. These limits are for Class D devices, which include personal computers, televisions and monitors. The harmonic amplitudes are proportioned to the input power of these devices. For lighting products, class C limits are applied, which are also proportional to input power and even more stringent. In the case of other products not used in such high volume, the limits are fixed at the values corresponding to 600 W input. The performance of the passive PFC, as shown in this graph, just barely complies with the limit for the third harmonic (harmonic number 3).

**Figure 1–6. Input Harmonics of Three PC Power Supplies Relative to IEC61000–3–2 Limits**
Passive PFC

Figure 1–7 shows the input circuitry of the PC power supply with passive PFC. Note the line-voltage range switch connected to the center tap of the PFC inductor. In the 230-V position (switch open) both halves of the inductor winding are used and the rectifier functions as a full-wave bridge. In the 115-V (switch closed) position only the left half of the inductor and the left half of the rectifier bridge are used, placing the circuit in the half-wave doubler mode. As in the case of the full-wave rectifier with 230 Vac input, this produces 325 Vdc \((230 \cdot \sqrt{2})\) at the output of the rectifier. This 325 Vdc bus is, of course, unregulated and moves up and down with the input line voltage.

![Passive PFC in a 250 W PC Power Supply](image)

The passive PFC circuit suffers from a few disadvantages despite its inherent simplicity. First, the bulkiness of the inductor restricts its usability in many applications. Second, as mentioned above, for worldwide operation, a line-voltage range switch is required. Incorporation of the switch makes the appliance/system prone to operator errors if the switch selection is not properly made. Finally, the voltage rail not being regulated leads to a cost and efficiency penalty on the dc-dc converter that follows the PFC stage.

**Critical Conduction Mode (CrM) Controllers**

Critical Conduction Mode or Transitional Mode (also known as Borderline Conduction Mode BCM) controllers are very popular for lighting and other lower power applications. These controllers are simple to use as well as inexpensive. A typical application circuit is shown in Figure 1–8.
The basic CrM PFC converter uses a control scheme (current mode control) similar to that shown above. An error amplifier with a low frequency pole provides an error signal into the reference multiplier. The other input to the multiplier is a scaled version of the input rectified ac line voltage. The multiplier output is the product of the near dc signal from the error amplifier and the full-wave rectified sine waveform at the ac input.

The signal out of the multiplier is also a full-wave rectified sine wave that is scaled by a gain factor (error signal), and is used as the reference for the input voltage. The amplitude of this signal is adjusted to maintain the proper average power to cause the output voltage to remain at its regulated value.

The current shaping network forces the current to follow the waveform out of the multiplier, although the line frequency current signal (after filtering) will be half of the amplitude of this reference. The current shaping network functions as follows:

In the waveforms of Figure 1–9, Vref is the signal out of the multiplier. This signal is fed into one input of a comparator, with the other input connected to the current waveform.

When the power switch turns on, the inductor current ramps up until the signal across the shunt reaches the level of Vref. At this point the comparator changes states and turns off the power switch. With the switch off, the current ramps down until it reaches zero. The zero current sense circuit measures the voltage across the inductor, which will fall to zero when the current reaches zero. At this point the switch is turned on and the current again ramps up.
As the name implies, this control scheme keeps the inductor current at the borderline limit between continuous and discontinuous conduction, or critical conduction. This is important, because the wave shape is always known, and therefore, the relationship between the average and peak current is also known. For a triangular waveform, the average is exactly one half of the peak. This means that the average current signal (Inductor current \( \cdot \text{Rsense} \)) will be at a level of one half of the reference voltage.

The frequency of this type of regulator varies with line and load. At high line and light load, the frequency is at a maximum, but also varies throughout the line cycle (high frequency near zero crossing and low frequency near the peak).

**Critical Conduction Mode without a Multiplier (Voltage Mode)**

A novel approach to the critical conduction mode controller is available in some ON Semiconductor ICs, most recent example being NCP1607. These chips provide the same input-output function as the controllers described above; however they accomplish this without the use of a multiplier [2].

As was explained in the previous section, the current waveform for a CrM controller ramps from zero to the reference signal and back to zero. The reference signal is a scaled version of the rectified input voltage, and as such can be referred to as \( k \cdot \text{Vin} \), where \( k \) is a scaling constant from the ac voltage divider, error amplifier and multiplier in a classic circuit. Given this, and knowing the relation of the slope of the inductor with the input voltage, the following are true:

\[
\text{Ip}_{\text{pk}} = k \cdot \text{Vin}(t) \quad \text{and} \quad \Delta I = \frac{\text{Vin}(t)}{L} \cdot t_{\text{on}}
\]

![Figure 1–10. CRM Current Envelope](image)

Equating the peak current for these two equations gives:

\[
k \cdot \text{Vin}(t) = \frac{\text{Vin}(t)}{L} \cdot t_{\text{on}}
\]

Therefore, \( t_{\text{on}} = k \cdot L \)

This equation shows that \( t_{\text{on}} \) is a constant for a given reference signal \((k \cdot \text{Vin})\). \( T_{\text{off}} \) will vary throughout the cycle, which is the cause of the variable frequency that is necessary for critical conduction. The fact that the on time is constant for a given line and load condition is the basis for this control circuit.

In the circuit of Figure 1–11, the programmable one-shot timer determines the on time for the power switch. When the on period is over, the PWM will switch states and turn off the power switch. The zero current detector senses the inductor current, and when it reaches zero, the switch is turned on again. This creates the same dc output as with the classic scheme, without the use of the multiplier. The benefit of the voltage mode CrM control is that the multiplier is not needed and the input voltage sensing network is eliminated. In addition, the current sensing is needed only for protection purpose.
Since a given value of on time is only valid for a given load and line condition, a low frequency error amplifier for the dc loop is connected to the one-shot. The error signal modifies the charging current and therefore, the on time of the control circuit so that regulation over a wide range of load and line conditions can be maintained.

One of the voltage mode CrM controllers, the MC33260 contains a number of other features including a circuit that will allow the output voltage to follow the input voltage. This is called follower boost operation (shown in Figure 1–12). In the follower boost mode, the output voltage is regulated at a programmed level above the peak of the input voltage. In most cases, the output of the PFC converter is connected to a dc-dc converter. Many dc-dc converter topologies (e.g. flyback converters) are capable of regulating over a wide range of input voltages, so a constant input voltage is not necessary. On the other hand, if a topology can not function well over a wide input range, the follower boost output range needs to be narrowed (if it is used).

Follower boost operation offers the advantages of a smaller and therefore, less expensive inductor, and reduced on-time losses for the power FET [3]. This is normally used in systems where the lowest possible system cost is the main objective.

**Frequency Clamped Critical Conduction Mode (FCCrM)**

Although the Critical Conduction Mode is widely used in the industry, it has some known limitations. The primary limitation being the variable switching frequency which reaches peak at light loads and also near the zero crossing of the sinusoid. Some solutions which clamped the frequency excursion by putting a maximum frequency clamp resulted in the distortion of current (since the Ton was not adjusted for this) and lower power factor as the inductor entered the discontinuous mode of operation. This is illustrated in Figure 1–13.