Dealing with PLL clock jitter in advanced processor designs

Part 2: Jitter Frequency Domain Transfer Function Through a PLL

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In this second of a three part series published on Embedded.com, engineers at Analog Devices, Inc. examine the sources of clock jitter in designs based on advanced RISC and DSP architectures, how to characterize your system for such problems and then how to resolve them.

Without a detailed discussion of PLLs (which, in itself, has little to do with the subject at hand), we can just state that a PLL, being a phase locked loop, is linear in phase and, thus, is linear in jitter.

Although this statement is not as simple as it looks, it is correct and we’ll leave it at that. This is good news, because linear systems can be analyzed in terms of their frequency domain transfer function (i.e., frequency response). Note that this transfer function is linear in jitter only. A PLL itself is certainly not linear as output with respect to input. Thus, the linear system discussion that follows looks at the transfer of jitter through the PLL only.

Generally, a PLL will have a fairly flat unity gain response up to a certain frequency (because a low-frequency jitter appears as a slowly varying phase that the PLL has enough time to adjust for). Also, as is the case with all real-life systems, frequency response rolls off at the high end. The locations of these cut-off points and the response between these cut-off points vary among PLLs. The jitter transfer function for ADSP-TS201S processors with a base clock of 125 MHz and PLL multiplier set to 4 is shown in Figure 2, below.
Another important factor in this analysis is: given a clock at the processor maximum allowed frequency, by how much can a clock period shrink before failure? In case of ADSP-TS201S TigerSHARC processors, this value is 40 ps (i.e., 2% of the 2 ns period of a 500 MHz clock).

Armed with this data, it is time to analyze jitter tolerance. We begin with sinusoidal jitter.

**Sinusoidal Jitter**

The sinusoidal jitter of amplitude $A$ (measured in time units, say seconds) and frequency $f$ (in Hz) is given by $J(t) = A \sin(2\pi ft)$. From the previous discussion, we know that $A$ is the TIE jitter.

This jitter inputs into the PLL of the ADSP-TS201S and outputs $J_f(t) = A(f) \sin(2\pi ft)$, where $A(f)$ are taken from the graph in Figure 2. According to formula (1), period jitter (which, stated above, must be less than 40 ps), is given by:

$$\max_{k=0,1,2,3,...} \left\| P_k - C_0 \right\|.$$  

Since $G$ of equation (7) is monotonically increasing, it is also invertible. The edges of $C_f(t)$ are at points $kT$, so the edges of
\[ C_{J+}(t) = C_T(G(t)) \]

are at points \( G^{-1}(kT) \). Thus,

\[ P_k = G^{-1}((k+1)T) - G^{-1}(kT) . \]

We now invoke the Intermediate Value Theorem from beginner calculus, which states that, given a continuously differentiable function, the difference of this function’s values at the end points of an interval equals the length of that interval times the derivative of the function at some point inside the interval. We thus obtain:

\[ P_k = \frac{d(G^{-1})}{dt}(t_0)((k+1)T - kT) = \frac{d(G^{-1})}{dt}(t_0)T \]

for some \( t_0 \in [kT,(k+1)T] \).

Again, using beginner calculus, if

\[ y = G^{-1}(t), \text{ then } t = G(y) \text{ and } \frac{dy}{dt} = \frac{1}{dt}, \text{ i.e.} \]

\[ \frac{d(G^{-1})}{dt}(t) = \frac{1}{\frac{dG}{dt}(y)} = \frac{1}{\frac{dG}{dt}(G^{-1}(t))} . \]

Substituting this into the above (with \( t = t_0 \)) gives:

\[ P_k = \frac{T}{\frac{dG}{dt}(G^{-1}(t_0))} . \]

Since \( G(t) = t - A(f)\sin(2\pi ft) , \)

\[ P_k = \frac{T}{1 - A(f)\cos(2\pi ft)_0)^2} \]

We now use Figure 2 to find the worst (i.e., maximal) value of \( A(f)f \). Note that the curve in this figure rolls off at the high end at the rate of 12 dB/oct. This means that every time we double the frequency, amplitude is divided by 4. Thus, \( A(f)f \) is maximized at the beginning of the roll-off curve (i.e., at approximately 7 MHz) where the PLL actually boosts the jitter amplitude by about 5 dB. Thus,

\[ \max_f \{A(f)f\} \leq 2^5 A \cdot 7 \cdot 10^6 = 12.46 \cdot 10^6 \cdot A . \]

Substituting this back into equation (8) gives:
\[ P_k \geq \frac{T}{1 + 2\pi \cdot 12.46 \cdot 10^6 \cdot A} \geq \frac{T}{1 + 79 \cdot 10^6 \cdot A} \text{, so} \]

\[ T - P_k \leq T - \frac{T}{1 + 79 \cdot 10^6 \cdot A} \]

\[ = \frac{79 \cdot 10^6 \cdot A \cdot T}{1 + 79 \cdot 10^6 \cdot A} \leq 79 \cdot 10^6 \cdot A \cdot T \]

The ideal clock input in this case is 500 MHz (125 MHz input multiplied by PLL by a factor of 4 (see Figure 2), so

\[ T = 2\text{ns} = 2 \cdot 10^{-9} \text{sec} \text{, then} \]

\[ T - P_k \leq 79 \cdot 10^6 \cdot A \cdot 2 \cdot 10^{-9} \leq 158 \cdot 10^{-3} A \],

which must be \(\leq 40\text{ps} = 40 \cdot 10^{-12} \text{sec} \).

Solving this inequality for \(A\) yields

\[ A \leq 0.253 \cdot 10^{-9} \text{sec} = 253 \text{ps} \].

Thus, in the case of sinusoidal jitter, to satisfy the 40 ps of period jitter required by ADSP-TS201S processors, we must ensure that the TIE of that jitter is no more than 253 ps. Unfortunately, one usually cannot assume that the jitter will be sinusoidal in nature, in which case the above analysis does not apply completely.

But it does show how estimating the absolute value of the derivative of the jitter relates TIE to period jitter. Note that the above analysis can be performed more simply, without referring to the derivative. The reason that we did it in the more complicated way is because most of this argument will apply when we analyze general case jitter. In Part 3 in this series of articles we will turn our attention to this more difficult case.

**In Part 3 of this series the authors cover “Guidelines for measuring TIE jitter.” The topic of Part 1 is “Defining clock jitter terminology.”**

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