RapidIO IP cores ready to provide a path to faster interface design

Charles Frazer explains how the RapidIO specification is playing its part in the design of multicomputer, embedded, communications, signal processing, and other low-latency high-performance systems.

The need for intellectual property (IP) cores has increased significantly as semiconductor gate counts have followed Moore’s Law, doubling roughly every 18 months. Yet manufacturers’ IP development schedules have remained static, forcing semiconductor companies to modify their design process by incorporating IP from internal and external sources in an effort to keep up with the abundance of available gates.

Compressed chip development schedules and increasingly larger chip sizes are requiring semiconductor vendors to rely heavily on IP vendors for standards-based IP and verification IP cores that simplify and speed development time in order to meet aggressive product schedules. Supporting the demand for IP are standards for quality, delivery and on-chip protocols, all designed to ease integration by semiconductor manufacturers.

Standards-based IP

The need by semiconductor manufacturers to have access to a broad range of IP has fueled the growth of many technologies and standards in the marketplace. For board- and chassis-level connectivity bus-stand- ard IP, such as PCI, RapidIO, HyperTransport and others, has had the greatest acceptance, as it enables external connectivity to standard interfaces and applies to numerous, diverse markets.

One example is the RapidIO standard, an established, scalable, open-standard, switched fabric, used by component manufacturers and OEMs in the wireless infrastructure, edge networking, storage, scientific, military and industrial markets. RapidIO is also one of the serial standards that is used widely in multicomputer, embedded, communications, signal processing, and other low-latency high-performance systems.

Heavily involved in the creation of these standards, many of the same companies are creating and marketing the RapidIO IP in order to leverage their in-depth working knowledge of the RapidIO protocol.

This IP fully implements the RapidIO protocol and is designed for use by semiconductor manufacturers who see the tangible benefits of incorporating reliable, high-performance RapidIO endpoints into their products.

Chips from a variety of vendors – native RapidIO endpoints from Freescale and Texas Instruments and RapidIO switches from Mercury Computer Systems, Tundra Semiconductor, and PMC-Sierra, for example – create an ecosystem that enables product developers to build complete systems.

This robust ecosystem is driving the creation of new chips based on RapidIO IP, which can come in the form of application-specific integrated circuits (ASICs) that add bridges that connect to other standards such as PCI Express and Ethernet, and processor buses such as AMBA and CoreConnect to the existing ecosystem of switches and endpoints. In addition, many low-volume custom requirements can be met with field-programmable gate arrays (FPGAs) that connect RapidIO to a variety of custom functions.

Secondary IP markets

When a critical mass of corporations embrace a new standard and a large enough investment of resources in silicon products takes place, a secondary market naturally emerges for other...
companies wanting to connect to the established infrastructure.

In the past, reaching critical mass has been hampered by the enormous effort and cost required to develop and test the IP before connecting it to a standard bus. This barrier is being dismantled by IP providers who offer a fully tested and validated IP core for incorporation into any silicon.

In the case of RapidIO, for example, companies can use an IP core to incorporate a RapidIO endpoint without the years of design and verification required to develop and test the IP. This barrier is especially useful in standard bus interfaces like RapidIO, because a significant amount of protocol knowledge is embedded within the tests.

When choosing a partner for verification testing, it is important to evaluate each vendor’s expertise in the protocol at both the specification and system levels, where users have gained extensive knowledge of the protocol in run-time systems.

Verification testing

Once a company has introduced a bus standard such as RapidIO into its design, it must be tested to ensure that the interconnection of the IP to the company’s core logic is correct. Verification IP is a crucial aspect of quickly and thoroughly testing the IP integration into the design. A typical system-level verification environment used to test the users design is shown in Figure 1. Many verification IP providers offer a set of standard-directed tests to prove basic functionality. This is especially useful in standard bus interfaces like RapidIO, because a significant amount of protocol knowledge is embedded within these tests.

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A verification environment should include the capability to easily generate tests, which can create traffic patterns that users would expect to see in the system. These tests, when randomized, allow extensive testing of the protocol IP to be integrated into the users’ design without a large time investment. If the verification IP and protocol IP are purchased from the same vendor, the integration time is shorter, better results are obtained, and communication is simplified by having a single point of contact.

**IP delivery standards**

The lack of standards for IP delivery has made the integration of external IP more difficult and time-consuming. This problem has been recognized by the industry and IP standards are being developed to fulfill this need. The Spirit Consortium, for example, is working on a new standard mechanism for delivering IP.

This consortium (www.spiritconsortium.org) is an industry-level cooperative that is developing specifications for IP description and tools. It has defined an XML-based flow that enables the IP provider to deliver documentation, configuration, HDL, and high-level behavioral information in a single standard.

The goal is to provide developers with enough information to program the EDA tools to integrate the IP into the chip in the best way with minimal effort. The decisions required to configure the IP can be extended to the verification IP, thereby allowing the verification IP to be configured to meet the exact needs of the design IP that was configured by the tool.

The IP marketplace is maturing quickly after years of lackluster performance. This growth is driven largely by the need for standards-based IP and verification IP cores that can significantly reduce the time and effort involved to include these standards in end products. The growth of IP and the ease of its integration are further enhanced by standards for IP quality, delivery, and on-chip protocols, such as the Virtual Socket Interface Alliance (VSA), The Spirit Consortium, and the OCP/IP trade organizations.

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