Got PFC?: Understanding Power Factor Correction
and the tradeoffs in the various approaches to implementing it

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Electronics are a part of everyday life. Washing machines, refrigerators, vacuum cleaners, fans, and incandescent light bulbs have long been commonplace in even the most modest homes. Add to that the mounting number of large-screen televisions, home-network and computer-related equipment, gaming systems and battery-charging devices such as cell phones, MP3 players and cordless tools found in many modern homes, and it’s easy to visualize the role each of us contributes to the growing economic energy crisis.

The combination of millions, or perhaps billions, of electronic gadgets loading down the electrical power grid world-wide has presented utility providers with an unprecedented challenge. In addition to the insatiable amount of power that must be provided to every residential and industrial customer, power quality is a dominant concern for utility companies.

Power factor (PF) is one measure of power quality, indicating how efficiently energy is drawn from the AC source. PF is defined as the ratio of real power in watts (W) to apparent power (product of root mean square (RMS) current and RMS voltage) in volt-amperes (VA).

Complex reactive loading introduces higher order current harmonics that distort the shape of the AC current. This necessitates a more detailed definition of PF which takes into account current displacement and harmonic distortion.

Equation (1) provides a definition of PF that accounts for current harmonic distortion, defined as distortion factor in Equation (2), and phase displacement, defined as displacement factor in Equation (3).

\[
PF = \frac{\text{Real Power (W)}}{\text{Apparent Power (VA)}} = \frac{P_{avg}}{V_{RMS} \times I_{RMS}} = \frac{I_1}{\sqrt{2}} \times \cos(\phi_1)
\]

(1)

Note that in Equation (1), the PF can never be greater than 1. Therefore unity PF occurs when the RMS current is limited to the fundamental frequency only (distortion factor = 1) and the displacement angle, $\phi_1$, is zero (displacement factor = 1).

\[
\text{Distortion Factor} = \frac{I_1}{\sqrt{2} \sum_{n=1}^{\infty} \frac{I_n^2}{\sqrt{2}}}
\]

(2)
Displacement Factor = \cos(\varphi)

\begin{align}
\text{PF} &= 0.321 \\
\text{PF} &= 0.991
\end{align}

\textbf{Figure 1. AC Circuit (a) without PFC and (b) with PFC}

To illustrate a practical example highlighting the effect of low PF, suppose that each of the 120V AC waveforms shown in Figure 1 was measured at a residential electrical outlet that was protected by a 15A circuit breaker. The AC current waveform shown in Figure 1b was measured while a load with internal, active PFC (PF=0.991) was drawing power from the AC line. Under these conditions, the circuit would be able to provide approximately 1.78kW of real power. Next, suppose the equipment with PFC is removed and replaced with a similar load not equipped with PFC and the AC current waveform shown in Figure 1a was measured. Due to the low PF of 0.321, the circuit would only be able to provide approximately 0.985kW of real power. The key point is that a low PF yields less real power, requiring higher RMS current, resulting in lower efficiency due to transmission line losses.

Aside from the obvious interest that utility providers have, where poor PF results in inefficient distribution of power, what is the motivation for manufacturers of consumer electronics to include PFC in their end products? Numerous government and industry mandates and guidelines exist pertaining to controlling current harmonics and meeting certain PF requirements in AC-DC power supplies. For example, EN61000-3-2 is just one of the more widely accepted specifications which originated in the European Union (EU). EN61000-3-2 imposes limits on the harmonic currents drawn from the AC source.

EN61000-3-2 is applicable to electrical and electronic equipment having an input current less than 16A.
per phase while operating from an AC source voltage greater than 220V AC. The EN61000-3-2 standard recognizes four classes of electrical equipment, each with varying degrees of harmonic limits that must be met. Although these requirements pertain only to products sold within Europe, a similar document, IEEE 519 and its amendments, exists for the United States. Power supply designers often use active PFC circuits in order to meet the harmonic requirements of specifications such as EN61000-3-2 and IEEE 519.

Active PFC is really just another switching regulator that appears after the EMI filter and the FW rectifier bridge and in series with a load or DC-DC converter. A simplified top level schematic of a PFC power stage is shown here in Figure 2.

![Figure 2. AC Circuit with PFC Power Stage and Downstream DC-DC](image)

The most popular power topology used in active PFC is the non-isolated boost converter comprised of inductor L1, MOSFET Q1, Diode D1, and the PFC bulk capacitor, Cb. The AC input voltage is first passed through an EMI filter network and then fed through a full wave (FW) rectifier. The rectified AC voltage serves as the input voltage to the PFC boost converter. The output voltage of the PFC boost, Vb, is a regulated DC voltage that is commonly used as the input voltage to a downstream DC-DC converter stage.

There are three different operating modes for the boost converter and each one is defined by the control method used to shape the boost inductor current. When the peak-to-peak inductor ripple current is intended to be greater than zero for every switching cycle, this is known as continuous conduction mode (CCM) operation.

When the peak-to-peak inductor ripple current is less than zero during any portion of the switching cycle, this is known as discontinuous conduction mode (DCM) operation. Normally, PFC converters are not intentionally designed to operate in this mode, but during fault conditions, light load, or near the zero crossing of the AC voltage waveform, DCM operation may be unavoidable. Allowing a converter to operate in DCM will increase harmonic distortion and lower PF.

When the inductor current is operated at or near the “boundary” just between CCM and DCM this is referred to as boundary conduction mode (BCM) or critical conduction mode (CRM) PFC. Depending on the output power level, CCM and BCM each have significant pros and cons, making one better suited than the other.

The CCM control technique is based upon a fixed frequency control algorithm that can be used at any power level. The inductor current waveform for a PFC converter using CCM control is shown in Figure 3.
Figure 3. CCM PFC Inductor Current Waveform

The average inductor current is shown by the dotted blue line in Figure 3 and should follow a (rectified) sinusoidal wave shape that is in phase with the input voltage. The lower peak-to-peak inductor current has several advantages: the peak to RMS current ratio is lower, reducing conduction losses; magnetic core losses are reduced; and EMI filter requirements can be reduced.

However, the CCM PFC suffers from reverse recovery loss associated with the output rectifier, D1, a consequence for maintaining continuous ripple current through the boost inductor. In an attempt to eliminate the problems associated with reverse recovery, a silicon carbide (SiC) diode can be used as the output rectifier. SiC diodes have extremely low reverse-leakage current and do not suffer from reverse recovery losses. They are available with voltage ratings in excess of 1kV and perform exceedingly well in CCM PFC applications. Their only drawback is higher cost compared to a standard silicon rectifier, which can be a difficult justification, especially for use in cost-sensitive consumer electronic applications.

For lower-power PFC applications, the BCM control technique offers significant performance and efficiency benefits unobtainable from CCM PFC. The most obvious difference between CCM and BCM is the variable-frequency control algorithm used for BCM. The variable-frequency BCM technique operates at higher frequency near the zero crossing while the lowest frequency operation occurs near the peak of the AC line voltage. The on-time is fixed within a given half line cycle but the off-time varies significantly within the same line cycle. The BCM inductor is also much smaller compared to a CCM design at the same power level, which results in higher peak currents. These high peak currents appear as core loss to the boost inductor and present a significant EMI problem when trying to use BCM at higher power levels. For this reason, the BCM technique is optimally considered for PFC applications with output-power requirements less than about 300W.

Switching Frequency Lowered for Illustrative Purpose

Figure 3.BCM PFC Inductor Current Waveform
The real benefit of BCM is the fact that the MOSFET turns on when there is zero current in the output rectifier. This also means that the reverse voltage is applied to the diode only after the current has reached zero so there are no reverse recovery losses in the output rectifier. Unlike CCM, a SiC diode is therefore not required for BCM so a lower-cost silicon power diode can be used.

For PFC power levels up to 300W, the BCM technique can achieve greater efficiency, but what if the benefits of BCM could be extended to higher-power levels through interleaving? Interleaving two BCM power stages retains all the benefits of single phase BCM and CCM without any of the downsides. BCM interleaving offers better thermal management by spreading out the power-stage components not associated with reverse recovery losses, smaller inductors, lower switching loss through ZCS and ZVS, and reduced ripple current at an effective frequency of twice the switching frequency. Performance results can vary, but depending on input-voltage range and EMI requirements, the dual interleaved BCM approach can be used at power levels up to 1kW.

However, interleaving two BCM-controlled PFC power stages is not straightforward. Synchronizing two BCM power stages, each operating at different varying frequencies, is a nearly impossible task to design discretely. In order to retain the ripple current cancellation benefits from a two-stage design, it is imperative that each channel be synchronized 180 degrees out of phase with respect to the other. Since each channel is ideally designed to process 50% of the power, disrupting or losing synchronization—especially any time the load exceeds 50% of the maximum rated current—can be catastrophic to the overall design. In other words, a synchronization algorithm lacking tight tolerance unnecessarily drives the need to over-design the power stage.

In an effort to meet efficiency, harmonic, and PF regulations, semiconductor manufacturers have responded by introducing control ICs targeting interleaved dual BCM PFC applications. One such solution is the FAN9612 from Fairchild Semiconductor, which solves the problem of synchronization using an innovative scheme called Sync-Lock™ interleaving technology. Besides guaranteeing synchronization during steady-state operation, Sync-Lock™ ensures precise 180-degree, out-of-phase operation during transient, start-up, and fault-recovery modes of operation, which is an important safety feature. In the case of a non-operating phase due to no ZCD detection, missing gate-drive connection (for example, no gate resistor), one of the power components failing in an open circuit, or similar errors, the operating phase is locked into fail-safe operation, preventing it from trying to deliver full power to the load.

In many cases, PFC must now be included in electronic equipment that historically never needed PFC. As a result, there has been an increasing demand for PFC-control ICs, with more sophisticated features, aimed at increasing efficiency and PF, providing advanced protection features and reducing overall component count. Interleaved BCM PFC controllers have gained wide acceptance because of their ability to extend the benefits of BCM to higher power levels, as shown in Figure 4.

In spite of the various system features provided, most PFC-control ICs use one of the three popular control methods discussed herein: CCM, BCM or interleaved BCM. Table 1 compares some of the more important pros and cons offered by each PFC-control technique.
Figure 4. PFC Product Offerings from Fairchild Semiconductor

<table>
<thead>
<tr>
<th>PFC Control Technique Comparison</th>
<th>Single BCM (CRM)</th>
<th>Interleaved BCM (CRM)</th>
<th>CCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>PF</td>
<td>+ Good</td>
<td>+ Good</td>
<td>+ Best</td>
</tr>
<tr>
<td>Efficiency</td>
<td>+ Good (lower power levels)</td>
<td>+ Best</td>
<td>+ Good (higher power levels)</td>
</tr>
<tr>
<td>Cost</td>
<td>+ Lower Cost (but also limited to &lt;300W)</td>
<td>+ Low Cost solution (300W-800W)</td>
<td>- Higher cost components to maintain high efficiency</td>
</tr>
<tr>
<td>Number of Components</td>
<td>+ Minimal</td>
<td>- Needs MOSFETs, 2 diodes, and 2 Inductors</td>
<td>+ Minimal to moderate</td>
</tr>
<tr>
<td>Inductor Size</td>
<td>+ Small</td>
<td>+ Smallest</td>
<td>- Biggest</td>
</tr>
<tr>
<td>Line Filter</td>
<td>- High peak currents → Larger line filter</td>
<td>+ Smallest line filter → Ripple current cancellation</td>
<td>+ Small line filter</td>
</tr>
<tr>
<td>Diode cost</td>
<td>+ Inexpensive Diodes</td>
<td>+ Inexpensive Diodes</td>
<td>- Need SiC / Hyper FR Diode</td>
</tr>
<tr>
<td>ZVS of MOSFET</td>
<td>+ ZVS ($V_{INAC} &lt; VO/2$) or Valley switching ($V_{AC}(t) &gt; VO/2$)</td>
<td>+ ZVS ($V_{INAC} &lt; VO/2$) or Valley switching ($V_{AC}(t) &gt; VO/2$)</td>
<td>- NA</td>
</tr>
<tr>
<td>Diode Reverse Recovery Loss</td>
<td>+ ZCS operation → No reverse recovery loss</td>
<td>+ ZCS operation → No reverse recovery loss</td>
<td>- Reverse recovery current → Higher switching loss</td>
</tr>
<tr>
<td>Current sensing loss</td>
<td>+ Small (lower threshold just for protection)</td>
<td>+ Small (lower threshold just for protection)</td>
<td>- Large (higher threshold for control)</td>
</tr>
<tr>
<td>Ripple Current</td>
<td>- Higher ripple current → Larger conduction loss</td>
<td>+ Smaller Ripple currents</td>
<td>+ Smallest Ripple Current</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>Variable Frequency</td>
<td>Variable Frequency</td>
<td>+ Fixed Frequency</td>
</tr>
</tbody>
</table>

Table 1. PFC Summary Comparison between BCM, Interleaved BCM and CCM
About the author

Steve Mappus is a Systems Engineer working in the High Power Solutions group at Fairchild Semiconductor (http://www.fairchildsemi.com). In his current role, he is responsible for new product development and definition of power-supply control ICs. He has more than 18 years of power-supply design experience, including 10 years designing military and commercial power systems for avionic applications.

More recently, he has spent the last eight years working in the power-management semiconductor business specializing in Systems and Applications Engineering. He has authored over 25 power electronic-design articles and application notes. His areas of interest include high-power converter topologies, soft-switching converters, synchronous rectification, high-frequency power conversion, and power-factor correction.