Understanding Factors Affecting Intel® QuickPath Interconnect Signal Integrity

ABSTRACT: The Intel® QuickPath Interconnect operates at extremely high frequencies and it is essential that circuit designers understand the myriad factors that affect differential signal integrity. This article introduces those factors and explains the basics of transmitting and receiving signals without significant distortion.

The objective of any electrical system design, from a signal integrity perspective, is to ensure that the signals transmitted by driving components are received without distortion significant enough to corrupt the data represented by those signals. For both parallel and serial-differential bus designs, the primary factors to consider and control are:

- Signal propagation or delay
- Crosstalk
- Reflective effects
- Signal attenuation or loss
- Jitter

Each of these is introduced in this article. Note that most of the factors discussed here apply both to Intel® QuickPath Interconnect (Intel QPI) and many other serial-differential (e.g. PCI Express™) and even single-ended interface designs.

Signal Propagation or Delay

Systems based on transmission lines have a certain physical delay associated with the time taken for signals to move from transmitter to receiver. Even in a lossless system, signals do not move instantaneously from one end of a system to the other. The time taken for the signals to traverse the system is called propagation delay.

Propagation delay is determined by the physical and electrical properties of the medium through which the signals move (that is, the dielectric of the material surrounding the signal-carrying wires and the physical dimensions of the wires themselves). For serial-differential systems, signal propagation delay is not a significant issue except where a specific timing relationship
must be maintained between data pairs, or between data and clock signals (for a notable exception, see the electrical chapter of the USB 2.0 specification). In the case of Intel QPI, both the Intel QPI specification and the individual platform design guidelines (PDGs) provide guidance on any critical timing relationships to maintain. In general, the absolute propagation time taken by Intel QPI signals is not constrained, though the relative time between some signals may be.

Crosstalk
Crosstalk is simply the impact of one signal on another. In the system context, this is due to electromagnetic coupling between signal-carrying media in close proximity. Crosstalk can occur in any medium, whether connector or cable routes, PCB or package traces or even vias. Crosstalk in a digital system is an AC phenomenon, appearing only when signals change state. The mechanisms for crosstalk are inductive coupling and capacitive coupling. In inductive coupling, one can consider the signal medium as a wire. As the signal changes state and therefore the amount of current through the wire changes, it generates a magnetic field. Any other wire-like structures in the generated magnetic field will “see” some amount of energy from the signal wire, as shown in Figure 1. The strength of the coupled magnetic field depends on the amount of energy in the wire and the distance between the victim wire and the signal wire.

Figure 1  Magnetic Field Coupling in a Differential Pair
Capacitive coupling is conceptually similar, except that the coupling mechanism is an electric field generated by the time-varying voltage in the signal wire, as illustrated in Figure 2. Again, any wire-like structure within the field will experience coupling effects whose strength is determined by the amount of energy in the original wire, the properties of the material separating the wires, and the distance between the wires.

![Figure 2 Electrical Field Coupling in a Differential Pair](image)

Crosstalk is a key concern in signal integrity, and the effects of crosstalk are usually captured by modeling the signal traces and their coupling effects directly, through a field solver. Crosstalk can increase or reduce the amount of cumulative signal seen at any particular time point (due to constructive or destructive interference, respectively). This can reduce voltage margin or timing margin or both.

**NEXT and FEXT**

For differential systems, near-end crosstalk (NEXT) and far-end crosstalk (FEXT) are important concepts, illustrated in Figure. These are often used to characterize multi-conductor systems such as cables and connectors. As implied by the name, NEXT is simply the crosstalk between a transmitting
signal and a neighbor, when both are measured at the transmitting (near) “end” of a differential system. FEXT is the crosstalk between a transmitting signal and a neighbor when the amount of energy on the neighbor is measured at the “end” of the system opposite the transmitter. In this way, both electromagnetic coupling and loss are included in the FEXT measurement. Some S-parameters data sets are called NEXT and FEXT, depending on the port orientation of the transmitter and interconnect “ends” (for example, a two-line, four-port system’s NEXT would be S13, if one line had ports 1 and 2 as its near and far endpoints respectively, with the other line having lines 3 and 4 as its endpoints, arranged similarly).

The impact of crosstalk can be included in an overall system budget (eye diagram, for example) used for simulation or validation. In the case of Intel QPI, the peak distortion analysis (PDA) technique accounts for overall topology crosstalk through Signal Integrity Simulation Tools for Advanced Interfaces (SISTAI), a web-based suite of tools provided for Intel customers. The simulation flow used to provide inputs to SISTAI assumes simulation of a three-pair, six-signal system, which will normally include...
crosstalk in the interconnects, including package, board, connectors, vias, and any other medium in which crosstalk has been modeled.

Reflective Effects
One of the primary problems affecting high-speed system designs is poor signal quality from reflections. Just as acoustical energy can “bounce” around a large room or wave fronts on the surface of a body of water can interact, electrical energy can reflect off of discontinuous areas in a signal path.

The problem with such interactions is that the energy from incoming and outgoing waves can constructively or destructively sum, causing apparent signal increases or attenuation, respectively. Should these effects occur at the receiver, the signal and therefore the data stream at the receiver can become corrupted or the receiver could be damaged.

In a concert hall, the placement of objects in the physical space and their sound absorption properties determine how the acoustical energy is perceived by the listener. If the space between the listener and the sound source is unobstructed and has uniform properties, and if the sound energy dies away before hitting the walls, the listener will perceive what the sound source generates without distortion, minus energy losses. Similarly, the placement and electrical properties of the system media determine the distortion of the signal at the receiver. The electrical impedance of the traces, vias, connectors, cables, and so on between the driver and receiver, plus the driver and receiver impedances themselves, have an enormous impact on the quality of the signal at the receiver.

Impedance, while a critical concept, is too large a topic to be addressed in depth here. Formally, impedance is the numerical relationship between time-varying electrical and magnetic fields. For the purposes of signal integrity, impedance is (as the name suggests) a quantitative measure of how easily time-varying signals pass into or through an electromagnetic medium.

In a system design where many different components may be connected (such as vias, traces, transmitters, receivers, and connectors), reflections occur when impedances of each of the connected components are mismatched. For example, a high impedance termination on a low impedance transmission line will cause significant amounts of energy to “bounce” off the termination and return to the driving signal source,
potentially causing significant distortions for current and subsequent data at the receiver.

When a system topology contains components or PCB segments with different impedances (such as backplanes and cards), reflections can result as the driven signal encounters the impedance mismatches and “bounces” between them. These reflections can destructively or constructively interfere with subsequent driven bits, respectively reducing or increasing the effective voltages per bit seen at the receiver. This phenomenon is called inter-symbol interference (ISI), because the data bits or symbols sent at one time cause difficulties interpreting later symbols.

Impedances can vary for many reasons. These include device variations, such as pad capacitance, package vertical path variations, and termination variance. These can also result from interconnect variations in sockets, PCB vias, and connectors. Finally, the PCB itself can contribute variations and mismatches, from layer transitions, and PCB-to-package and PCB layer-to-layer variations over high volume manufacturing (HVM). As described later, equalization of the driven bit pattern can reduce the ISI of the system by adjusting the driven voltages according to the anticipated topology and output bit pattern.

For most purposes, the ideal approach is to match impedances from component to component in a system signal path, or at least to tune the component impedances to reduce signal distortions at the receiver.

Impedance Matching

For the most part, trace impedance is the most malleable impedance of any component in a PCB system. Device and connector impedances are controlled by their respective manufacturers. Via impedances will be constrained by PCB stackup and manufacturing choices. Trace impedances, however, can be controlled through geometry decisions even if stackup and material choices have already been taken.

Single-ended characteristic impedance (hereafter, simply impedance) in a PCB trace is determined by its physical properties, including the dimensions of the trace and its distance from its reference. The material properties of the dielectric material and the trace itself are also critical. As a simple approximation, the impedance of a trace in a lossless sense can be computed from the capacitance of the trace with respect to its reference, and the inductance of the trace-reference loop, in the following equation:
where Zo is the impedance in ohms per unit length, Lo is the inductance in henries per unit length and Co is the capacitance in farads per unit length. Note how this neatly conveys how impedance is a relationship between electrical and magnetic fields—inductance represents the magnetic field contribution while capacitance represents the electric field contribution. More precise impedance information for individual components, including loss effects, can be determined from measurement or simulation.

In differential PCB systems, two impedance relationships should be managed: differential and common-mode. As with single-ended impedance, differential and common-mode impedances are determined by the physical and material properties of the traces and trace medium. However, common-mode impedance need not be managed directly. By controlling both the differential impedance of the trace pair and the single-ended impedances of each line in the pair, the common-mode impedances will be constrained. This will become obvious from the equations used to determine differential and common-mode impedances.

The differential impedance characterizes the relationship within a signal pair where the signal lines are switching in opposition (or odd mode, where voltages are complementary). The potential difference between the signals in the pair imply capacitive coupling separate from the capacitance of each signal to any nearby reference (PCB systems usually involve some reference plane as close or closer to the signals as the signals are to each other) as shown in Figure 4.

![Simplified Representation of Capacitive Coupling](image)

**Figure 4**  Simplified Representation of Capacitive Coupling
A common mathematical treatment of differential impedance for a pair of identical traces is
\[ Z_{\text{diff}} = 2 \cdot Z_{\text{odd}} = 2 \cdot (Z_{11} - Z_{12}) \]
where all the impedances are in ohms, \( Z_{11} \) is the single-ended impedance of either of the traces, and \( Z_{12} \) is the impedance of signal 1 to signal 2, neglecting effects of any nearby reference plane.

Common-mode impedance characterizes the relationship of the pair’s signals when they both switch in an identical fashion (voltages are identical). The lines therefore have the same potential relative to any reference, and any capacitive coupling effects between them therefore vanish.

A common mathematical treatment of common-mode impedance for a pair of identical traces is
\[ Z_{\text{common}} = \frac{Z_{\text{even}}}{2} = \frac{(Z_{11} + Z_{12})}{2} \]
where all the impedances are in ohms, \( Z_{11} \) is the single-ended impedance of either of the traces, and \( Z_{12} \) is the impedance of signal 1 to signal 2, neglecting effects of any nearby reference plane. One key reason these equations are at best simplifications is that PCB traces, as well as other devices, have frequency-dependent impedances, usually expressed in real and imaginary or other equivalent terms. As a result, matching may be possible only over a limited frequency range.

Again, the primary objective behind determining and controlling differential and common-mode impedances is to ensure that discontinuities are minimized between areas of interconnect. Reflections and attendant negative effects will therefore be reduced or eliminated. Note that impedances may not always be matched across the entire interface to achieve optimum signal integrity performance. While the Intel QPI system target impedance is 85 ohms, PCI Express for server platforms tends to combine 85-ohm interconnects with 100-ohm devices for optimum signal integrity. This is primarily due to the physical design parameters needed to achieve 85-ohm differential target impedances in typical systems. For typical computer systems, races are usually wider in 85-ohm designs than in 100-ohm designs, and dielectrics may also be thinner. While thinner dielectrics may actually increase dielectric loss, this shortens any via stubs. Similarly, wider traces will reduce the copper losses through the traces.
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