Dynamic Power Dissipation Considerations for Solid State Relays

*Understand the key attributes of this all-electronic switching component and how to take advantage of them*

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**Abstract**

For low-voltage signaling applications, or low-power switching applications, the optically isolated solid state relay (SSR) with MOSFET outputs provides significant advantages against the traditional electro-mechanical relays (EMR). One of the primary challenges that a designer faces using such relays is to determine and establish the maximum dynamic and static power dissipation experienced in the relay package.

The frequency of operation ultimately imposes an upper limit on the total power dissipation. Therefore, it becomes imperative that both dynamic and static power dissipation be accurately calculated such that the maximum power dissipation allowed for the SSR is not exceeded. This article also looks at some typical and interesting application examples where the SSR can be used in end applications.

**SSR dynamic-power dissipation calculations**

The instantaneous drain-to-drain voltage $v(t)$ and drain current $i(t)$ are both assumed to change in a linear fashion during the switching-time interval $T_{sw}$, **Figure 1**. This linear transition change is an approximation, but is good enough for all practical purposes.

![Figure 1: SSR switching: timing diagram](image-url)
The instantaneous power dissipation of the SSR (Figure 2) during the switching interval can be expressed as:

\[ p(t)_{\text{sw}} = v(t) \cdot i(t) \]  
Eq (1)

If a linear approximation is invoked, \( v(t) \) and \( i(t) \) are assumed to be a linear functions of time, as indicated in figure above. As such:

\[ p(t)_{\text{sw}} = \left[ \frac{V_d (T_{\text{sw}} - t)}{T_{\text{sw}}} \right] \cdot \left[ \frac{(I_d) (t)}{T_{\text{sw}}} \right] \]  
Eq (2)

In the expression above, the beginning of the switching cycle is assumed to be at \( t = 0 \). Also, the figure above indicates that the switching takes place at a frequency \( f \) with a time period of \( T_p \).

Simplifying Equation (2):

\[ p(t)_{\text{sw}} = \frac{\{(V_d) (I_d) (T_{\text{sw}}-t) (t)\}}{T_{\text{sw}}^2} \]  
Eq (3)

It is now possible to calculate the average power dissipated over the switching time interval \( T_{\text{sw}} \):
\[ P(T_{sw}) = \frac{1}{T_{sw}} \int_{0}^{t=T_{sw}} v(t) \cdot i(t) \, dt \quad \text{Eq (4)} \]

Combining equation (3) with (4):

\[ P(T_{sw}) = \frac{(V_d)(I_d)}{T_{sw}^3} \int_{0}^{t=T_{sw}} (T_{sw}-t) \, t \, dt \]

Solving the above integral yields the average power dissipation through the switching period \( T_{sw} \) is:

\[ P(T_{sw}) = \left[ \frac{(V_d)(I_d)}{6} \right] \quad \text{Eq (5)} \]

We are now able to readily calculate the Total Average Power Dissipation in a time period \( T_p \). Note that \( T_{sw}(1) \) is the fall time \( t(f) \) transition of the output of the SSR, and \( T_{sw}(2) \) is time \( t(r) \) or rise time transition of the output of the SSR:

\[
P \left( \text{Total Average over } T_p \right) = \left[ \frac{(V_d)(I_d)}{6} \right] T_{sw}(1) / T_p + \left[ \frac{(V_d)(I_d)}{6} \right] T_{sw}(2) / T_p + \left[ \frac{(R_{on})(I_d)^2}{T_p} \right] t(\text{on-state}) / T_p + \left[ \frac{(V_d)(I_{off})}{T_p} \right] t(\text{off-state}) / T_p \quad \text{Eq (6)}
\]

Since, \( f = 1/T_p \), the above equation can be formulated in terms of frequency, and substituting \( T_{sw}(1) = t(f) \) (output fall time of the SSR), and \( T_{sw}(2) = t(r) \) (output rise time of the SSR) as:

\[
P \left( \text{Total Average over } T_p \right) = \left[ \frac{(V_d)(I_d)}{6} \right] t(f) / f + \left[ \frac{(V_d)(I_d)}{6} \right] t(r) / f + \left[ \frac{(R_{on})(I_d)^2}{T_p} \right] t(\text{on-state}) / f + \left[ \frac{(V_d)(I_{off})}{T_p} \right] t(\text{off-state}) / f \quad \text{Eq (7)}
\]

Note: Equation (6) underscores that if the \( T_{sw} \) is small compared to the time period \( T_p \), the power dissipated during the switching period is relatively small. This is explained in the below. Equation (7) also underscores that as frequency increases, the fraction of power dissipated over the switching period \( T_{sw} \) also increases, and ultimately imposes the frequency limit of operation.

**Input Power Dissipation**

Average input power dissipated over a time period \( T_p \) is:

\[ P(\text{input}) = \left[ (V_f \cdot I_f) \right] t(\text{on state}) / T_p \quad \text{Eq (8)} \]

or in terms of frequency:

\[ P(\text{input}) = \left[ (V_f \cdot I_f) \right] t(\text{on state}) / f \quad \text{Eq (9)} \]
Practical Example for Calculating Power Dissipations

The ASSR-1510 solid state relay is being used to switch a load of 1A at a Vd of 60V. The switching frequency is 100 Hz at a duty cycle of 50%. The input drive current of the SSR is 5mA.

(a) Calculate the output power dissipation, input power dissipation, and total package power dissipation.

From the ASSR-1510 data sheet:

Vf (max) = 1.7V
Frequency (f) = 100 Hz,
R(ON) = 0.5 Ω

t(f) = output fall time = 200 μsec (estimated, because this is not a data sheet parameter)
t(r) = output rise time = 2 μsec (estimated, because this is not a data sheet parameter)

Time period Tp = 1/f = 10 msec
50% duty cycle means that t(On state) = 5 msec
t(Off state) = 5 msec

From Equation (7):

\[ P(\text{Total Average over } Tp) = \left[ \frac{(Vd) (Id)}{6} \right] t(f) (f) + \left[ \frac{(Vd) (Id)}{6} \right] t(r) (f) + \left[ R(ON) (Id)^2 \right] t(\text{on-state}) (f) + \left[ (Vd) (Ioff) \right] t(\text{off-state}) (f) \]  

---------Eq (10)

Calculating each of the above power dissipation components separately:

a) \[ \left[ \frac{(Vd) (Id)}{6} \right] t(f) (f) = \left[ \frac{60V \times 1A}{6} \right] \times 200 \mu\text{sec} \times 100 \text{ Hz} = 200 \text{ mW} \]
b) \[ \left[ \frac{(Vd)(Id)}{6} \right] t(r) (f) = \left[ \frac{60V \times 1A}{6} \right] \times 2 \mu\text{sec} \times 100 \text{ Hz} = 2 \text{ mW} \]
c) \[ \left[ R(ON) (Id)^2 \right] t(\text{on-state}) (f) = 0.5\Omega \times (1A)^2 \times 5 \text{ msec} \times 100 \text{ Hz} = 250 \text{ mW} \]
d) \[ \left[ (Vd) (Ioff) \right] t(\text{off-state}) (f) = 60V \times 1 \mu\text{A} \times 5 \text{ msec} \times 100 \text{ Hz} = 30 \mu\text{W} \]

Adding the above power dissipation components, gives the total output power dissipation as 452 mW.

The Input power dissipation is calculated from Eq (9):

\[ P(\text{input}) = \left[ (Vf \cdot I_f) \right] t(\text{on state}) (f) = 1.7 \times 5 \text{ mA} \times 5 \text{ msec} \times 100 \text{ Hz} = 4.25 \text{ mW} \]

Thus, total average package power dissipation per switching period is:

\[ = 4.25 \text{ mW} + 452 \text{ mW} = 456.25 \text{ mW} \]
This power dissipation is lower than the absolute maximum allowed for ASSR-1510 (540 mW). Therefore, the operating conditions do not require any power de-rating.

**The FET Driver and SSR**
The FET driver within the SSR is powered through photo-voltaic power alone, [Figure 3](#).

![Figure 3: FET Driver and Solid State Relay Functional Diagram](#)

The LED photo-flux received by the FET driver is the only energy that powers the FET driver to drive the output MOSFETs. The photovoltaic voltage is generated by a stack of twelve photodiodes stacked one on top of the other. Each photodiode generates approximately 0.5V (typical), and hence the total voltage generated by the photo-diodes is 0.5 x 12 = 6V (typical).

The amount of photocurrent generated is the peak current that charges up the combined gate capacitance of the output MOSFETs. The larger this photo-current is, the faster the gate voltage will be that is charged to the photodiode-stack photovoltaic voltage. Typically, this photo-current generated by the stack voltage is approximately in the range of 20 μA typical at a LED drive current of 10mA.

Within the FET driver design is a Fast Turn-Off circuit. The purpose of this circuit is to instantaneously discharge the gate capacitance once the SSR has been turned OFF by bringing the LED current to zero. This circuit just momentarily turns on when the photovoltaic voltage is collapsing. This fast turn-off circuit then guarantees the turn-off time of the SSR is much shorter than the turn-ON time of the SSR. The power dissipated in the FET driver is negligible, as the photo-current generated is typically 20 μA at a drive current of 10mA, and the stack voltage generated is approximately 6V (typical) at a drive current of 10mA.
The Avago Technologies FET driver design also encompasses Output Transient Reject circuit that assures a very high dVo/dt parameter and capability in the data sheet. The principle of operation of this circuit is that when the SSR is in the off-state, any transient high voltage perturbation on the contacts of the SSR is capacitively coupled into the base of the transient reject transistor, that momentarily turn-ON, and keeps the gate discharged and guarantees the output MOSFETs do not turn-ON when this transient high voltage pulse is received by the output contacts of the SSR.

5.0 Application Examples for the Solid State Relays

There are many applications for SSRs. Below the ("About the Author" section are some typical circuits, showing solar-cell-array battery charging (Figure 4), telephone pulse-dialer interface (Figure 5), a relay-coil driver (Figure 6), a temperature controller (Figure 7), and a multichannel AC load-control module (Figure 8).

About the author

Jamshed N. Khan, from Lahore, Pakistan has a BSEE in electrical engineering from the University of California, Berkeley. From 1979 to 1984, he worked at the Fairchild Semiconductor Company (Mountain View, California) as an analog designer and front-end manufacturing product engineer.

In 1984 Jamshed joined the Hewlett-Packard Company (Palo Alto, California) as yield enhancement and product engineer for the optical devices, including optocouplers and optically coupled solid state relays, then became an Applications Engineer for the optocoupler devices and joined the IEC 60747 SC47E/WG4 as a technical contributor and participant to generate an international safety standard IEC 60747 (for optocouplers and optically coupled solid state relays).
* Isolation diode prevents battery discharge into the solar array when SSR is off through any parasitic resistance or leakage current of the SSR.

Figure 4: Solar-cell-array for battery charging

Figure 5: Telephone pulse-dialer interface
Figure 6: Relay-coil driver

Figure 7: Temperature controller
Figure 8: Multichannel AC load-control module