New digital, capacitive isolators raise the bar in high-performance

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Tightening legislation for designing machinery and equipment in industrial and medical applications enforces the implementation of galvanic isolation into almost any type of electronic system or circuitry.

While digital isolators have largely replaced analog isolators, thereby simplifying the design of isolated interfaces, designers are now challenged with the continuously increasing demands towards higher system performance. Here high-performance not only stands for high data rates and/or low-power consumption, but also high reliability. On one hand this is accomplished through robust data transmission in harsh industrial environment. On the other, and in particular with regards to isolators, it is through longevity.

Recent technical advances in chip design and manufacturing have yielded a second generation of digital, capacitive isolators whose high-performance defines new benchmarks for low-power consumption and high reliability. This article explains their functional principle and internal construction, and discusses their current consumption and life expectancy.

Function Principle

Figure 1 shows the internal block diagram of a digital, capacitive isolator (DCI). The isolator input splits into two differential signal paths, a channel for high data rates, called AC-channel, and a channel for low data rates, named DC-channel. The AC-channel transmits signals between 100 kbps and 100 Mbps, and the DC-channel covers the range from 100 kbps down to DC.

![Figure 1. Internal block diagram of a digital capacitive isolator.](image)

A high-speed signal is processed by the AC-channel where first it is converted from single-ended into differential mode, and then differentiated into transients by the capacitor-resistor network of the isolation barrier. The following comparators convert the transients into differential pulses, setting and resetting a NOR-gate flip-flop. The flip-flop output resembling the original input signal feeds a decision-logic (DCL) as well as the output multiplexer. The DCL consists of a watchdog timer that measures the duration between signal transitions. If the duration between two
consecutive transitions exceed the timing window, as in the case of low-frequency signals, the DCL initiates the output multiplexer to switch from the AC to DC-channel.

Because low-frequency signals require large capacitors making on-chip integration difficult, the input of the DC-channel possesses a pulse-width modulator (PWM), which modulates the low-frequency input signals with the high-frequency carrier of an internal oscillator (OSC). The modulated signal is processed the same way high-frequency signals are processed in the AC-channel. Before submitting the signal to the output multiplexer, however, it is necessary to filter out the high-frequency PWM carrier through a final low-pass filter (LPF) to recover the original, low-frequency input signal.

One major advantage of the capacitive isolator over other isolator technologies is that its DC-channel presents the correct input polarity at the isolator output during power-up and during a loss-of-signal (LOS) event. Other isolator technologies lacking these features often show output glitches during power-up, or remain stuck to the last input polarity prior to signal-loss.

Internal Construction

Figure 2 shows a simplified diagram of the internal construction of a single-channel, capacitive isolator. Internally the isolator consists of two chips: a transmitter and a receiver chip. The actual isolation barrier is provided through the high-voltage capacitors located on the receiver chip.

Because the AC- and the DC-channel use a differential signaling technique to provide high noise immunity during data transmission, a total of four isolation capacitors are necessary to complete a single, isolated data channel.

![Diagram of internal construction of a single-channel capacitive isolator](image)

The right diagram in Figure 2 shows the cross section of a high-voltage capacitor. Bond wires leaving the transmitter chip attach to the aluminum top plate of the capacitor on the receiver side. The bottom plate, also aluminum, connects to the receiver logic. Between the plates is the inter-level dielectric, a 16-μm thick level of silicon dioxide (SiO₂).

The benefits of using SiO₂ as inter-level dielectric are twofold. First, it is one of the most robust isolation materials with the least aging effects and, therefore, extends the life time expectancy of capacitive isolators well beyond those of competing technologies. Second, SiO₂ can be processed using standard semiconductor manufacturing, thus contributing to significant lower production costs.

Further merits of capacitive isolation are the ultra-low capacity of 123 femto Farad (123 x 10⁻¹⁵ F) per capacitor, allowing transmission of very high data rates, and the tiny capacitor geometries that enable the production of multi-channel isolators.

Current Consumption
Isolator current consumption strongly depends on the internal construction. When comparing dual isolators, the inductive type appears to have the lowest DC supply current (Figure 3). This is because the device contains only two signal channels. The capacitive isolator, however, contains four channels: two AC and two DC. Thus, its current consumption at DC is higher, but so is its reliability by assuring the correct output polarity in the case of an input signal loss.

DC currents occur when systems are idling. Fortunately, industrial data acquisition systems, PLCs, and digital and analog I/O modules are not designed for idling, but for transferring data from sensors to control units and from control units to actuators. They must do this fast, reliably, and continuously.

Typically, dual isolators are used in isolated CAN and RS-485 bus nodes, where only the two data lines (transmit and receive) require isolation. An RS-485 transceiver, for example, must be able to provide a drive capability of up to ± 70mA under worst common-mode conditions to be standard compliant. Then, even at low data rates, the difference between DC currents becomes negligible.

When comparing quad isolators, the picture improves. While inductive isolators double in current consumption due to twice the amount of channels, the channel count for a four-channel capacitive isolator increases only by one versus the dual version. The reason for this is that only one DC-channel is used, which is multiplexed across four AC-channels (Figure 4). While the DC channel still provides high reliability, the total current consumption is kept at a minimum, thus increasing only marginally over the two-channel version.
Quad isolators are used to isolate interfaces comprising data and control lines, such as SPI, with data rates typically reaching from 20 to 80 Mbps. Current consumptions between inductive and capacitive isolators already differ by more than 10mA at, 30 Mbps, at higher data rates such as 100 Mbps, the difference is a spectacular 40mA.

Therefore, it really isn’t the DC-current that is of interest, but rather the increase of current over data rates, or the slope ∆i/∆f.

Life Expectancy

The life expectancy of an isolator is determined by the time-dependent dielectric breakdown (TDDB), which is an important failure mode for dielectric materials like silicon dioxide. Because of impurities and imperfections due to manufacturing, dielectrics deteriorate over time. This deterioration is accelerated by applying an electric field across the dielectric and by increasing its temperature.

Determining life expectancy is based on the TDDB E-model, which is the most widely accepted model for dielectric breakdown.

Practically the TDDB is determined by applying a stress voltage across the isolator, while maintaining the ambient temperature at 150°C (Figure 5). The start of the test activates a timer, which stops when the current through the isolator exceeds 1 mA, indicating a dielectric breakdown. The time-to-failure is noted for each test voltage and plotted against the theoretical E-model curve.

![Figure 5. TDDB test methodology.](image)

The TDDB curves in Figure 6 show that the test data for capacitive isolators, taken over a time frame of five years, perfectly match the E-model predictions, thus yielding a life expectancy of 28 years at a working voltage of 400 Vrms (560 Vpk), while the life expectancy for inductive isolators is < 10 years at the same voltage. The TDDB curves also reveal that between 700 V and 2.5 kV, the life times of capacitive isolators are about 10 times longer than those of inductive isolators.
Figure 6. Life time expectancies for capacitive and inductive isolators.

With industry lifetime expectations ranging from 10 to 30 years, capacitive isolators using SiO₂ dielectrics represent the only viable solution accomplishing that goal.

Conclusion

Digital capacitive isolators excel in performance through high reliability, low current consumption, large band width and long life times. Texas Instruments provides a wide range of digital, capacitive isolators including isolated bus transceivers and the new ISO74xx generation of capacitive isolators.

References


About the Author

Thomas Kugelstadt is a Senior Applications Engineer at Texas Instruments where he is responsible for defining new, high-performance analog products and developing complete system solutions that detect and condition low-level analog signals in industrial systems. During his 20 years with TI, he has been assigned to various international application positions in Europe, Asia and the U.S. Thomas is a Graduate Engineer from the Frankfurt University of Applied Science.