Introduction

In June 2009, NXP Semiconductors introduced a new portfolio of high-speed data converters (see http://www.nxp.com/#/homepage/cb=[t=p,p=/50935/53500] for more information). These data converters offer resolutions from 12 to 16 bits, single channel and dual channel options, and three different digital interface options including JEDEC JESD204A serial. JEDEC JESD204A (2008), to which NXP Semiconductors was a contributor, is a new industry standard for the interconnection of data converters and logic devices which supports the concept of multiple synchronously bonded serial data lanes. The technical details of this new data converter interface standard is the subject of this article.

The advanced feature set enabled by the low overhead JEDEC JESD204A digital interface presents a new design-in option for high-speed data acquisition engineers across the electronics industry. JESD204A is supported by industry standard FPGA families, including Xilinx’s Spartan and Virtex product families, Lattice’s ECP2M and EPC3 product families, and Altera’s Arria and Stratix product families.

1.0 JEDEC JESD204A Serialization

In April 2008, the JEDEC Solid State Technology Association JC-16 Committee on Interface Technology published the JESD204A specification, which is a significant revision to the JESD204 specification, published in 2006.

The key enhancement offered by JESD204A is the support beyond single lane links, to multiple time-aligned (synchronized) lanes per link. This enhancement enables the use of much higher bandwidth data converters, as well as multiple synchronized data converter channels. Specifically, the JESD204 specification, with only one lane defined at 3.125 Gbps, limits a single-channel 16-bit data converter to (3.125 Gbps/20) = 156.25 MSPS and limits a dual-channel 16-bit data converter to 78.125 MSPS.

JESD204A allows a single-channel data converter to multiplex its digital I/O across multiple lanes. For example, a 16-bit single-channel ADC multiplexing its output across four lanes has the potential to support a maximum sampling rate of ((3.125 Gbps/20) * 4) = 625 MSPS.

The use of a high-speed serial interface brings the additional benefit of IC package I/O pin reduction. For example, using conventional parallel LVDS I/O, a dual-channel 14-bit ADC requires (2 * 14) = 28 interconnect wires. By comparison, JESD204A defines a differential data lane, consuming two interconnect wires, each with (3.125 Gbps/10) = 312.5 MB/sec of maximum raw link bandwidth.

Following typical open systems models, the JESD204A specification includes an electrical PHY layer protocol, a transport layer protocol, and a data link layer protocol, and as noted above, adds an important new capability to the existing JESD204 specification: the ability to support multiple time-aligned lanes in a single data link protocol structure. JESD204A also allows a single ASIC (including DSPs and microcontrollers) or FPGA to support multiple (or “multipoint”) links, Figure 1.
The scope of JEDEC JESD204A is constrained to the interactions between one logic device (FPGA or ASIC) and one or more converter devices (ADC or DAC).

Time-aligned synchronization of two or more ADC channels or DAC channels is a requirement in many data acquisition systems, particularly in modern communications systems. For example, many wireless communications systems such as GSM/GPRS/EDGE cell phone systems rely on quadrature sampling techniques to reduce the minimum Nyquist sampling frequency and thus the bandwidth of the data processed by the downstream digital baseband processor, with the goal of reducing power, PCB area and BOM cost. In multi-carrier communications systems, such as those based on OFDM (including 3GPP Long Term Evolution, IEEE 802.11 and IEEE 802.16) fundamentally rely on quadrature sampling and on the preservation of precise phase information in the transmitter and receiver. OFDM systems must preserve phase coherency at the sample level for the digital signal processing algorithms to be valid. In the past, communication system engineers had to use proprietary synchronization techniques (typically involving shallow FIFOs and state machines) at the board-level to guarantee quadrature sample synchronization. The JEDEC JESD204A specification is intended to address this commonly found technical requirement, and foster interoperability among data converters and commonly used logic devices such as FPGAs.

2.0 The JESD204A Physical Layer

Note that data converters typically utilize a low pin count control/status bus to configure and monitor the functional characteristics of the JEDEC JESD204A interface; the details of control and status register interfaces are explicitly outside the scope of the JEDEC specification.

The JESD204A electrical PHY layer defines a SERDES-based differential serial protocol which is unidirectional and point-to-point, operating with self-clocked 8B/10B coded data at rates from 312.5 Mbps to 3.125 Gbps. Transmitter devices (ADCs or FPGAs/ASICs) and receiver devices (DACs or FPGAs/ASICs) on the same FR-4 printed circuit board are guaranteed to operate up to 3.125 Gbps on copper traces at least 20 cm in length with full signal integrity if the PHY implementation is compliant to the JESD204A specification.

Transmitters and receivers can also be on separate PCBs connected through a backplane with impedance-controlled connectors or through shielded twisted-pair cables with impedance-controller connectors. JESD204A compliant devices are not required to support the full data rate range of
312.5 Mbps to 3.125 Gbps. Note that the link bandwidth range 312.5 Mbps to 3.125 Gbps includes the 8B/10B encoding overhead, so the actual payload data transfer rate is lower.

8B/10B encoding has the dual merits of utilizing a computed “running disparity” to maintain DC balance (zero DC offset) in the electrical signal (allowing the signal to be high-pass optically, capacitively or inductively coupled) and the ability to detect single-bit errors at the receiver. The running disparity is a continuously computed binary value (interpreted as either “+” or “−”) that enables the 8B/10B state machine to select one of two appropriate output bit patterns (called a “valid code group” in the spec) to maintain long-term DC balance.

The electrical signalling defined by JESD204A is low-swing/low-voltage and differential. It complies with what is widely known as CML (Current Mode Logic), used in the DVI and HDMI standards for digital audio and video transmission. Consistent with CML, JESD204A specifies 100-ohm transmission line termination at 1.2V. JESD204A compliant transmitters and receivers must achieve a Bit Error Rate (BER) of less than $10^{-12}$. Transmitters and receivers may be either fully DC-compliant or AC-compliant only. AC-compliant only devices must be coupled with external capacitors. This standard also defines transmit and receive eye diagram masks and related jitter specifications to which compliant devices must conform.

JESD204A defines three logical signals per link. The first logical signal is the lane, which is the differential 8B/10B self-clocked encoded CML signal. The second logical signal is the frame clock, which is the shared clock signal for sequencing control and data frames and maintaining the frame alignment. The low-voltage frame clock is distributed to all transmitter and receiver devices connected to the link (all data converters and the FPGA/ASIC logic device).

The frame clock (or a multiple / sub-multiple) is also generally used as the data converter sample clock, the absolute timing reference for the transmitter / receiver system, and must exhibit low jitter (including both random and deterministic jitter contributions). Because of this low jitter requirement, the frame clock should not be derived from the recovered serial data link clock at the receiver. Note that the frame clock may be implemented as a differential pair (LVDS or CML). The third logical signal is the active-low SYNC~, which is a time-critical return path hardware signal from the JESD204A DAC/ASIC receiver (or receivers) to the ADC/ASIC transmitter (or transmitters) that indicates when the link must be initially synchronized, periodically resynchronized or when a data error has occurred.

SYNC~ must be synchronous with respect to the frame clock input to the transmitter, and the JEDEC specification includes propagation delay, setup and hold time requirements. Note that SYNC may be implemented as a differential pair (LVDS or CML). In systems with multiple DAC devices (i.e., separate chips), the individual SYNC~ signals must be combined (logically ORed typically) into a single logical subsystem SYNC~, and presented to the FPGA/ASIC transmitter (more on this below). SYNC~ signal skew must be managed by the system designer; the JESD204A specification includes several tables of requirements for skew management. Figure 2 and Figure 3 are illustrations of generic example multipoint ADC and DAC links.
Figure 2 – ADC Multipoint Link Generic Example
It is, in part, by virtue of the fact that there is a single frame clock and a single logical SYNC~ per JESD204A subsystem that sample time-alignment (and thus precise phase coherency) is possible among the data lanes.

Note that the JEDEC JESD204A standard does not address itself to the lane-to-lane synchronization of multiple DAC devices (separate DAC IC packages), which is required for precise analog output phase alignment. The standard assumes the multiple DACs will be similar components from the same data converter manufacturer, so the specification of the inter-device, lane-to-lane synchronization mechanism is left open for innovation, though it is assumed to operate at the frame clock rate, and the user is not expected to have to provide a separate clock.

It is logical to assume that data converter vendors would employ the same lane-to-lane synchronization mechanism used inside single package devices with multiple lanes and multiple DACs, and publish the details necessary for this mechanism to be used at the board level. The JEDEC JESD204A specification assumes this mechanism would not necessarily be interoperable between DAC vendors.

Note that in the JEDEC JESD204A specification, the link connecting a logic device (FPGA, ASIC, processor) with multiple ADCs or DACs is called a “multipoint link”. This terminology is potentially
confusing (“multipoint” in this usage is not synonymous with “multi-drop”), as the JESD204A standard defines a point-to-point interconnect (one transmitter is always connected to just one receiver). The specification also defines four device classes: NMCDA-SL (No Multiple Converter Device Alignment – Single Lane); NMCDA-ML (No Multiple Converter Device Alignment – Multiple Lane); MCDA-SL (Multiple Converter Device Alignment – Single Lane); and MCDA-ML (Multiple Converter Device Alignment – Multiple Lane).

2.0 The JESD204A Transport Layer

There are several mapping options defined in the JESD204A specification: a single converter to a single-lane link; multiple converters in the same device to a single-lane link; a single converter to a multi-lane link; and multiple converters in the same device to a multi-lane link. As mentioned above, the JESD204A standard also allows the system designer to combine multiple converter devices on a multipoint link.

The JESD204A transport-layer framing-state machine groups samples and/or partial samples into frames of 8-bit “octet” data structures. The standard allows more than one sample per converter to be transmitted per frame cycle, with the constraint that the number of samples per converter per frame must be an integer, in order to minimize crosstalk between the SERDES digital circuits and the analog circuits.

In this specification, a “sample” is defined as N data bits plus optional control bits (such as over-range indication bits) plus optional tail bits. The tail bits are used at the end of the frame to fill out or pad out a whole number of octets per lane per frame cycle. Interestingly, the specification points out that constant value tail bits can cause spurious spectral lines if optional scrambling is not used. The use of pseudo-random tail bits is recommended. The spec also recommends the use of pseudo-random dummy bits during idle mode.

The JESD204A transport layer maps samples to words (potentially adding control bits such as over-range indication) which are mapped to extended words (potentially adding tail bits to fill-out or pad-out 4-bit nibble groups, and, if necessary, adding tail bits to make the total number of bits a whole multiple of 8), which are mapped to 8-bit octets. The first user data octet transmitted in time corresponds to the most significant byte; the second user data octet transmitted in time corresponds to the least significant byte. Figure 4 illustrates the basic dual ADC transmit signal chain, and Figure 5 illustrates the basic dual DAC receive signal chain.
Figure 4 – Dual ADC Transmit Signal Chain

Figure 5 – Dual DAC Receive Signal Chain
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