Revolutionary Architecture for the Next Generation Platform FPGAs

Embargoed News:
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The Evolution of FPGA Architectures

- 1985: FPGA for glue logic
- 1987: FPGA for core functionality
- 1992: FPGA w. soft system IP
- 2001: Logic Platform w. hard & soft system IP
- 2002: System Platform w. Processor IP
- 2004: Domain-specific Platforms
The ASMBL™ Architecture

Application Specific Modular Block Architecture

Column Based ASMBL Architecture

Feature Options
- Logic
- DSP
- Memory
- Processing
- High-speed I/O
- Hard IP
- Mixed Signal
- Future...

Domain A
- Applications

Domain B
- Applications

Domain C
- Applications

Future
- Applications
Addressing Geometric Constraints

- I/O and array dependency
- Power & ground distribution
- Hard IP scaling
ASMBL Addresses
I/O and Array Dependency

Array increase, I/O increase

Array constant
I/O increase

Array increase, I/O constant

Peripheral I/O
dependent on array size

Column based I/O
independent of array size
ASMBL Addresses
PWR & GND Distribution

• New Pwr & Gnd distribution reduces voltage drop
• Switching reliability increase via higher thresholds
ASMBL Addresses
Hard IP Scaling

Array size increase to accommodate feature scaling

Array size constant as features scale independently

Traditional Architecture

ASMBL Architecture
ASMBL Advantages

• Xilinx Benefits
  – Reduces time & risk for FPGA platform development
  – Enables cost-effective assembly of multiple platforms
  – Allows rapid response to new market demands

• Customer Benefits
  – Highest value solution at a given price point
  – Right feature mix for a given domain
ASMBL Enables Domain-Specific Platforms

Right feature mix at the lowest cost
Cost Effectively Expanding Xilinx FPGA Application Domains

Next Gen Virtex Domain A

Next Gen Virtex Domain B

Expand beyond traditional $5.1B PLD Market

Next Gen Virtex Domain C

Next Gen Virtex Domain D

Virtex-II Pro

Virtex-II

Virtex-E

Virtex

Market Data Source: Gartner Dataquest 2007 Projection FPGA/CPLD Market
Taking Advantage of Moore’s Law

Transistor count increases, cost decreases
Taking Advantage of 10+ Layers of Metal

Metal Layers

10+
10
9
8
7
6
5
4
3
2
1


Next Gen Virtex

Virtex-II Pro

Virtex-II

Virtex-E

Virtex

ASMBL

Granularity

IP

Immersion

Substrate
Taking Advantage of Advanced Packaging

- Flip Chip enables column based architecture
- Allows connecting to I/Os anywhere on the die
- Enhanced thermal dissipation

Package source: Amkor Technology
Next Generation Cost Metrics

Cost per Function

Old density based metrics
$/LC and $/Gate

New capability based metrics
$/MAC/s or $/BOPS
$/Mbit of storage
$/Gbps bandwidth
$/Gbyte/s bandwidth
$/DMIPS
$/system functionality
$/mixed signal
Conclusion

- ASMBL enables domain-specific Platform FPGAs
- Addresses traditional architectural limitations
- Highest value solution at a given price point