Circuit lets you test sample-and-hold amplifiers

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Sample-and-hold amplifiers sample an analog voltage and hold it until an ADC can digitize it. A perfect sampling circuit holds a voltage until digitizing is complete. Thus, the amplifier's output is identical to its input. Real sample-and-hold amplifiers, however, can gain or lose voltage, producing an error. Offset voltages in amplifiers cause a static additive error. Further, there occurs a specific additive error, the so-called voltage pedestal, which originates within the transition from the sample state to the hold state because of a parasitic charge transfer to the hold capacitor.

A sample-and-hold amplifier uses an analog switch to connect a signal to a holding capacitor. When the switch closes, thus having low resistance, the capacitor charges to the sampled input voltage. During the hold time, when the switch has high resistance, the sampling capacitor holds the voltage until the ADC digitizes it. During the transition from low to high switch resistance, a parasitic charge injection, mainly from the gate of the switch to the hold capacitor, continues to charge the capacitor until the switch's control voltage reaches a steady logic level. The injected charge produces an error voltage at the capacitor. Additional errors may occur during the hold time. Leakage and bias currents in the amplifier combine with tens of picocamps of leakage current in the switch and capacitor to cause the capacitor to charge or discharge during hold time.

By applying a logic-control signal with a duty cycle of $D$ and $1-D$, you can measure a mean output voltage difference, $[\Delta V_{OUT}] = [V_{OUT} - V_{IN}]$, which is the peak voltage drop. Leakage and bias currents in the amplifier combine with tens of picocamps of leakage current in the switch and capacitor to cause the capacitor to charge or discharge during hold time.

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$[\Delta V_{STAT}] = V_{STAT} + D V_{INJ} + \frac{1}{2} D V_{DROPPEAK}$, where $\Delta V_{OUT}$ and $\Delta V_{INJ}$ are the output-voltage differences for $D$ and $1-D$, respectively; $V_{STAT}$ is the steady output-voltage difference for a selected value of the reference input voltage, $D$ is the duty cycle, $V_{INJ}$ is the voltage pedestal, and $V_{DROPPEAK}$ is the peak voltage drop. Figure 1 shows how the voltages in the equations change over time. If you apply a complementary control waveform with a duty cycle of 25%, you can measure another dc component of the sample-and-hold amplifier's output voltage. Finally, when the sampling switch is continuously on, you can measure the $V_{STAT}$ voltage, which is a real dc voltage. $V_{OUT}$ and $V_{INJ}$ contain a waveform superimposed onto a selected value of the reference voltage. Thus, you should measure the mean voltages using a series resistor with a value of, say, 10 kΩ.

Multiplying the voltage pedestal, a simple rectangular waveform, by the duty cycle yields the av-

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$\text{Figure 1}$ A sample-and-hold amplifier’s holding capacitor experiences a voltage drop due to leakage and bias currents plus a voltage step, which results in a difference between the amplifier’s output and input voltages.
erage value. In contrast, the voltage-drop waveform appears as a sawtooth. Its mean rises as one-half of the duty cycle squared. The peak-voltage-drop value denotes a hypothetical voltage drop at the end of a whole period, T, of the SAMPLE/HOLD logic-control waveform.

You can use the previous equations to find the values of the voltage pedestal and the peak voltage drop. A 75% duty cycle is a convenient value. The following equations are valid for this duty cycle: $V_{\text{INJ}} = 6[V_{\text{OUT}} - 2/3V_{\text{STAT}}] - 16/3V_{\text{STAT}}$ and $V_{\text{DROPPEAK}} = 16[-[V_{\text{OUT}} - 2/3V_{\text{STAT}}] + 1/3[2V_{\text{STAT}}]$. You must find the optimal repetition rate, $f_{\text{REP}}$ of the logic-control signal. As the optimal repetition rate increases, the difference in output voltage from the input is almost purely due to dc voltage offset plus the voltage pedestal: $(V_{\text{OUT}} - V_{\text{STAT}})/(V_{\text{OUT}} - V_{\text{STAT}}) = 3$. The following equation finds the maximum value for the optimal repetition rate: $f_{\text{REP}} = (0.01/4) \times 1/(t_{\text{on}} - t_{\text{off}})$, where $t_{\text{on}}$ and $t_{\text{off}}$ are the on and off times, respectively. This equation ensures that the difference in values between the turn-on and turn-off times of the sample-and-hold amplifier’s internal analog switch won’t affect the accuracy of the precision 25 and 75% duty cycles by more than 1%.

If you evaluate the equation for a high-performance analog switch, such as the Analog Devices (www.analog.com) ADG1213, you get a repetition rate of 33 kHz or less. The difference due to voltage drop prevails at low-value repetition rates. In this case, the repetition rate can be the value of the frequency at which $V_{\text{OUT}} - V_{\text{STAT}} = 1/10 \times V_{\text{INMAX}}$, where $V_{\text{INMAX}}$ is the maximum input-voltage range. The best way to determine the lower limit of the repetition rate is through experimentation.

A tested sample-and-hold amplifier using the circuit in Figure 2 uses a supply voltage of −1 V, a drain-to-drain voltage of 5 V, and a supply voltage of 3.3 V for logic circuits in the pulse generator. Two sets of measurements at 25, 75, and 100% duty-cycle values for the AGD1213’s internal switch control used input voltages of 0 and 2.5 V. You will measure the output-voltage difference, approximately −0.0366 mV, and the pedestal voltage, approximately −0.0333 mV, at a repetition rate of 1.762 kHz. The value of the residual effective charge injection, $Q_{\text{INJ}}$, into the hold capacitor, $C_h = 2 \text{nF}$, is $Q_{\text{INJ}} = C_h \times V_{\text{INJ}}$. The value is negative and doesn’t exceed −75 fC. The following equation defines the difference of charge injection within the 2.5 V range of input voltage: $\Delta Q_{\text{INJ}} = Q_{\text{INJ}}(2.5 V) - Q_{\text{INJ}}(0 V)$ and yields a value of −6.7 fC. The following equation determines the residual effective leakage current from the acquired values of peak voltage drop at a repetition rate of 160 Hz: $I_{\text{LEAK}} = C_h \times V_{\text{DROPPEAK}} \times f_{\text{REP}}$, where $I_{\text{LEAK}}$ is the leakage current. A leakage current at the input voltage of 0 V is approximately 17 pA, and a leakage current at the input voltage of 2.5 V is approximately −17 pA.

**Reference**


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**Add hysteresis to a voltage comparator**

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Positive feedback is a typical technique for distributing hysteresis around a comparator, provided that you have a resistive path between the comparator’s output and the noninverting input. Positive feedback forms two threshold voltages that have (or assume) fixed values. In addition, they depend on the saturation values of the comparator’s output stage. Plus, the load conditions affect their accuracy. The circuit in Figure 1 provides an alternative for applications requiring a comparator with hysteresis that has precise thresholds that you can easily and independently set. The circuit includes two inverting and noninverting threshold comparators whose outputs directly drive a set/reset latch. You can use a latch with either active-low or active-high inputs.

You can generate the positive and negative threshold voltages using a...
precision voltage reference that powers a resistor divider (not shown) or by driving the inputs with DACs if you need a digitally programmable comparator. The circuit’s high input impedance facilitates this task. Because of its hold state, the latch nullifies the effects of frequent switching on the comparator’s outputs due to noise on the input signal. The circuit thus acts as a Schmitt trigger even if there is no positive feedback. The latch introduces a propagation delay that’s normally a few tens of nanoseconds and is negligible in low- to medium-speed applications. Because the latch has complementary outputs, the circuit provides a noninverting characteristic on the Q output and an inverting characteristic on the Q̅ output (Figure 1a and b).

Some integrated latches have only the Q output. If you need an inverted output, you need only to exchange the comparator outputs with the latch inputs for both circuits; the upper comparator drives the reset input, and the lower comparator drives the set input. You can use open-collector or open-drain comparators to process bipolar or positive signals higher than the supply voltage of the latch. You can easily interface them without using clamping diodes. You must add only a pullup resistor that the logic supply powers.

The circuit uses IC1, an STMicroelectronics (www.st.com) dual micro-power comparator with a push-pull output stage. In this case, the supply voltage must be the same as that for the latch.Edn

**Broken-coil detector is simple yet robust**

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The circuit in this Design Idea was originally designed to detect damaged conveyor belts in the mining industry. Thin coils are embedded in the conveyor belt. If the belt suffers damage, it stretches at the affected location, causing one or more coils to break. The method for detecting the broken coil is to allow a “sensing” coil to magnetically couple with the passing coils in the belt, thus changing the total inductance of the magnetic pair. The sensing coil is part of an LC oscillator (Figure 1). When an intact coil passes the sensing coil, the frequency of the oscillator changes. If the conveyor belt moves at a fixed speed, the frequency of the oscillator modulates...
at a fixed rate. When a broken coil passes the sensing coil, there is more time between modulations (and this is what you want to detect).

The oscillator doesn’t generate a pure sine wave and is power-hungry but stable. It oscillates over a large range of LC pairs, even with a low quality factor and with almost any transistor. The amplitude is flat across a large bandwidth. The frequency is \( \frac{1}{(2\pi \sqrt{L_1 C_1})} \), where \( L_1 \) is the inductance of the sensing coil. \( R_2 \) represents its resistance. \( L_2 \) and switch \( S_1 \) represent either undamaged or broken coils in the conveyor belt. When \( S_1 \) is closed, the coils are undamaged, and when \( S_1 \) is open, the coils are broken. When the coupling between the sensing coil and a conveyor coil is perfect, it is equivalent to having the two connected in parallel, which would reduce the total inductance and increase the frequency of oscillation.

The problem now becomes how to detect different frequencies by implementing an FM demodulator or frequency-to-voltage converter. An easy way to accomplish this task is to pass the signal from the oscillator through an appropriately tuned lowpass filter. If the frequency range of the oscillator lies at the beginning of the roll-off, a higher frequency causes higher attenuation. At this point, an FM waveform has become an AM waveform, which you can easily demodulate using envelope detection.

You can experimentally determine the best value for the threshold. You can perform the comparison with an analog comparator or with a microcontroller after digitizing the signal. This last method would allow you to measure the time since the most recently detected undamaged coil passed.

Figure 1 shows that by using a filter comprising \( R_5 \) and \( C_4 \) and driving the envelope detector comprising \( D_1 \), \( R_6 \), and \( C_3 \), you can check at the output of this circuit to see whether the voltage is above or below a certain threshold. You can experimentally determine the best value for the threshold. You can perform the comparison with an analog comparator or with a microcontroller after digitizing the signal. This last method would allow you to measure the time since the most recently detected undamaged coil passed.

Figure 2 shows a trivial RC lowpass filter comprising \( R_5 \) and \( C_4 \) and driving the envelope detector comprising \( D_1 \), \( R_6 \), and \( C_3 \). To find out whether the sensing coil couples to an external coil, you can check at the output of this circuit to see whether the voltage is above or below a certain threshold.

Figure 3 shows a second-order lowpass filter that removes ripple from the envelope detector’s output.
Figures 3 and 4 show a simple and reliable analog method, using the envelope signal, to detect that a bad coil has passed. The output from the envelope detector contains ripple, so lowpass filtering allows a more precise discrimination in frequency. In this example, the filter in Figure 3 makes the ripple insignificant without deteriorating the frequency response of the system.

The output of the filter then feeds into the comparator (Figure 4). $R_{14}$ sets the threshold, which should be at the midpoint between the generated voltages with and without an external coil coupled to $L_1$, $D_2$, $C_6$, $R_{12}$, and comparator IC$_6$ behave as a countdown timer set to a time slightly longer than the period between passing coils. $C_6$ quickly charges to a maximum voltage when a good coil passes and then slowly discharges. If the time between (sensed or detected) consecutive undamaged coils is below a certain maximum, the voltage across $C_6$ should never go below the threshold that $R_{15}$ sets, thus keeping the output of IC$_6$ low and lighting LED $D_3$. If a damaged coil passes, the oscillator’s frequency should remain the same, allowing the voltage across $C_6$ to drop enough to trigger the comparator, turning off the “all-good” light.

In a real-world application, you should latch the output to ensure that the operator notices the alarm condition. The circuit could simply shut down the power to the conveyor belt, allowing immediate repairs and indicating where the fault occurred. The circuit uses just a few common components with large tolerances on their values. Its use of transistors, op amps, discrete linear and nonlinear components, oscillators, filters, demodulators, converters, and magnetically coupled circuits make it an excellent teaching resource. It even gives some insight into how modern proximity-card technologies, such as RFID (radio-frequency identification) work.EDN

**Figure 4** Comparator IC$_6$ monitors the voltage across $C_6$ and activates when the $C_6$ voltage exceeds a preset value from $R_{15}$. 

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**Diagram**

- FROM SECOND-ORDER LOWPASS FILTER
- $V_{CC}$
- $V_{CC}$
- $V_{CC}$
- $R_{11}$
- $1k$
- $D_2$
- $+$
- $IC_6$
- $R_{14}$
- $1k$
- $D_3$
- $5V$
- $-$
- $C_6$
- $R_{12}$
- $R_{15}$
- $+$
- $IC_6$
- $V_{CC}$