NOTE:
ABM3I2: LIMIT [(6.28 mF/µF) × (V(IN1) + V(IN2)) + 2 × CMRR)], −1m × V(IN3)/(2 × IB), 1m × V(IN3)/(2 × IB).

Figure 2 These op-amp model input stages model the input-bias currents of NPN (a) and PNP (b) transistor inputs.