When processing signals from analog sensors, you frequently encounter wide variations in attenuation among communication channels or sensors. Or, you face situations in which several identical sensors within a supervised system return signals of roughly similar spectral composition and dynamic range but with considerably different maximum amplitudes. Sometimes, it’s possible to predict these and other variations and adjust the gain of preprocessing amplifiers. More frequently, you encounter unpredictable signals and thus lose data associated with nonrepeatable events. In these circumstances, an adaptive preamplifier with AGC (automatic gain control) can prevent measurement-channel saturation and data loss.

AGC preprocessing suppresses the absolute amplitude of a sensed signal while preserving the best possible resolution of individual spectral components’ relative amplitudes. The circuit in this Design Idea offers one relatively simple and efficient approach to per-channel AGC. The circuit uses a method of direct low-level signal control using a short-circuited bipolar transistor. In Figure 1, a variable voltage divider comprising a fixed resistance, $R_1$, and a variable resistance controls the signal’s ac amplitude. The variable resistance comprises the differential resistance of a bipolar transistor, $Q_1$, short-circuited from base to collector. To vary $Q_1$’s resistance, you force direct current into the shorted transistor from a current source comprising voltage source $V_{REG}$ and a high-value resistor, $R_2$. To prevent $R_1$ from affecting the circuit’s ac-voltage-transfer characteristic, $R_1$’s resistance must greatly exceed $R_2$’s.

For all reasonable values of positive current I—generally, less than the transistor’s maximum rated emitter current ($I_E$)—transistor $Q_1$’s collector-to-emitter saturation voltage is less than its base-emitter threshold voltage, and the transistor operates in the active state. The shorted transistor’s VI (voltage-versus-current) characteristic curve strongly resembles that of a PN diode and follows Shockley’s Equation except for slightly higher dc-voltage values. That is, the device’s voltage variation is proportional to the logarithm of the dc-current variation.

Therefore, the shorted transistor’s differential resistance at every dc operating point along the VI curve is inversely proportional to the passing dc current; in other words, the device’s differential conductance is directly proportional to the current. Because, in its active state, a common-emitter-connected bipolar transistor’s current-amplification factor is typically 100 or more, the differential resistance accurately follows this rule over a broad range of currents.

Thus, varying $V_{REG}$ in Figure 1 varies the current, I, and controls the $R_1Q_1$ voltage-division ratio. Coupling capacitors $C_1$ and $C_2$ separate the...
circuit’s attenuator from the input-signal source and output load. Figure 2 illustrates a typical small-signal bipolar transistor’s short-circuited VI characteristic, showing that you can control differential resistance over at least five decades of range—that is, more than 100 dB.

In a practical circuit, the finite values of $R_1$ and $R_2$ limit the control range. For proper operation and to keep the signal’s THD (total-harmonic-distortion) factor, $k$, below 5%, the output-voltage amplitude, $V_{OUT}$, should be just a few millivolts. Even with these limitations, this attenuator circuit appears to offer one of the best and simplest AGC circuits.

Figure 3 shows the completed circuit design. The input signal, $V_{IN}$, drives buffer stage $Q_1$, whose unbypassed emitter resistor, $R_3$, serves four purposes. First, it increases $Q_1$’s differential output resistance to the approximate value shown in Equation 1:

$$R_{DI} = \frac{h_{1E} + h_{2E}R_3}{h_{1E}h_{2E}}$$  (1)

The increase in the circuit’s differential output resistance is so large that the value of $R_4$, 27 kΩ, almost exclusively determines the overall output resistance. Second, leaving $R_1$ unbypassed reduces $Q_1$’s voltage gain to:

$$A_{IC1} = \frac{h_{2E}R_3 - h_{2I}R_4}{(R_3 + R_4)D_{he} + \left[h_{2E} + 1 - h_{12E} + (R_3 + R_4)\right] R_3 + h_{11E}} = -\frac{R_4}{R_3}$$  (2)

This equation simplifies to $A_{IC1} \approx \frac{-R_4}{R_3}$. (Note that $P_{he}$ denotes the determinant $(h_{1E}h_{2E} - h_{11E}h_{2I})$, which this Design Idea includes for theoretical accuracy. However, you can neglect the numerical value of $D_{he}$ for modern silicon transistors without significantly affecting the calculation’s accuracy.)

Third, as Equation 2 shows, leaving $R_1$ unbypassed helps linearize the response of $Q_1$’s collector current-to-voltage drive. Fourth, $Q_1$’s differential base input resistance rises to:

$$R_{IBASE} = h_{1E} + h_{2E}R_4$$

which is larger and less dependent on $Q_1$’s instantaneous operating point than $h_{11E}$ alone.

In Figure 3, resistor $R_4$ forms the variable attenuator’s fixed resistance, analogous to the upper resistor, $R_1$, in Figure 1, and $Q_4$ forms the attenuator’s variable-resistance element. Transistor $Q_5$ supplies $Q_4$’s collector-drive current, and $Q_5$’s common-emitter configuration.
tion draws little base current. This approach enables use of a high value for AGC-release time-determining resistor R17, thus permitting a long AGC-release time. Resistor R19 limits the maximum dc control current through Q5 and Q6.

The large value of C3, when you compare it with Q6’s minimum differential resistance—that is, its maximum signal amplitude—at full control, presents negligible reactance to the lowest frequency-signal-spectrum component. A voltage-doubler rectifier comprising D1 and D2 extracts a portion of the signal from output stage Q4 and produces the control voltage for Q5. This arrangement accommodates both polarities of large peak amplitudes of nonsymmetrical signal waveforms. Resistor R15 determines the AGC’s “attack” time. Too small values of R15 in combination with C6 can lead to instability by creating a pole in the feedback-transfer function. Resistor R17 determines the AGC-release time.

To secure good response to high-frequency-signal components, use either Schottky or fast PN silicon diodes for D1 and D2. The dc-coupled complementary cascade comprising Q2 and Q3 supplies most of the circuit’s voltage gain. A 1-kΩ resistor, R14, isolates Q4, the output-emitter follower, from the signal-output terminal. If necessary, you can use a lower resistance at R14, but a large-capacitance connecting cable can provoke Q4 into parasitic oscillation if R14 is too low.

Figure 4 shows the circuit’s input-versus-output characteristics as measured with a sine-wave signal. The effective AGC range extends from 100-μV to 100-mV-rms input voltage, a 60-dB dynamic range. Output voltage varies less than 2 dB over this input range, reaching a nominal level of 775 mV rms at a −20-dB (100-μV-rms) input level. The input’s 0-dB point is set arbitrarily at 1-mV-rms input, which corresponds to an 803-mV-rms output. The AGC attack time for a sinusoidal input-signal step from 0 to 100 mV rms is approximately 0.3 sec, and the AGC release from 100-mV-rms input to −20 dB (100-μV rms) is approximately 100 sec. Figure 4 also includes a graph of THD versus input voltage. The distortion is well below a 5% THD limit throughout the input-voltage range. To measure the attenuator’s baseline input noise, terminate the input with its nominal 1-kΩ source resistance. At low input voltages, input stage Q1’s noise limits the processed signal’s usable dynamic range. The rms noise level is about −38 dB relative to the nominal output for input signals below the AGC threshold. When the AGC becomes active, the SNR increases in proportion to the AGC reduction. For example, with a 0-dB (1-mV-rms) input signal, the SNR increases to approximately 60-to-1.

If you assemble the circuit using the passive-component values in Figure 3, the amplifier’s −3-dB bandwidth spans 45 Hz to 35 kHz. At a power-supply voltage of 9 V, no-signal current consumption is approximately 12 mA. Figure 5 shows a photograph of the assembled pc board.
Precision active load operates as low as 2V

By Joel Setton, Crolles, France

This Design Idea presents a self-powered, precision-active-load circuit that improves on a previously published design (Reference 1). Added features include a wider operating-voltage range of 2 to 50V or higher and several flexible current-setting modes. The circuit in Figure 1 uses National Semiconductor’s LM10, which suits this application. The LM10’s reference section, IC1A, generates a precision 1.2V reference, which VS establishes. As a result, Q3 provides.

Transistor Q3 acts as a current mirror of transistor Q2’s collector current and supplies power to shunt regulator Q1. Resistors R9 and R7 set the current-mirror ratio, and the current through resistor R9 depends on the current through R7, which VS establishes. As a result, Q7, which mirrors the collector current of Q2, provides power to the shunt regulator. VS sets R6, which determines the load current as follows:

On Range A, the load current varies at 1A per turn of P1—that is, 10A maximum with P1 set fully clockwise. On Range B, the load current varies at 100 mA per turn of P1—that is, 1A maximum with P1 set fully clockwise. On Range C, an external voltage source that connects to R13 controls the load current at a rate of 1A per volt with P1 set fully clockwise. You can drive the external input with a function generator to test a power supply’s transient response. On Range D, the load circuit emulates an adjustable power resistor with load current proportional to the voltage across the load’s terminals. The equivalent resistance varies with P1’s setting—that is, \( R_{LOAD} = 100\Omega / \text{NTURNS} \) for a 100-mA output current. Then, rotate P1 fully clockwise and adjust R20 to set the output current to 1A. Repeat these two adjustments in sequence because they interact slightly. Current that IC1 draws through Q3 sets the minimum current through the load circuit at slightly less than 1 mA.

Because the circuit operates at 2 to 50V, it is suitable for testing the low-voltage outputs of a PC’s power supply. You can extend the maximum voltage by selecting suitable transistors for Q2, Q3, and Q4 through Q8; the LM10’s regulated power-supply voltage does not link to the external voltage. Note that when dissipating large amounts of power, transistors Q6 and Q7 require adequate cooling to maintain safe junction temperatures.

To calibrate the circuit, connect it to a suitable power supply delivering any voltage from 2 to 50V. First, set P1 to one turn—that is, one-tenth of full-scale—and S1 to Range B. Adjust R17 for a 100-mA output current. Then, rotate P1 fully clockwise and adjust R20 to set the output current to 1A. Repeat these two adjustments in sequence because they interact slightly. Current that IC1 draws through Q3 sets the minimum current through the load circuit at slightly less than 1 mA.

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REFERENCE

Squeeze extra outputs from a pin-limited microcontroller

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Many of today’s designs use low-cost microcontrollers from Freescale and Microchip, but during the last decade, device packages have resorted to ever-smaller footprints featuring as few as eight or even six pins. Although these packages minimize pc-board area, they also reduce the number of available I/O pins and pose problems for designers who need to add one more function without migrating to a device that occupies a larger package.

To overcome a shortage of inputs, a designer can increase a small microcontroller’s inputs by writing a program that multiplexes and polls the input pins. However, this approach doesn’t lend itself to extending outputs, because most designs require simultaneously driving multiple pins. Figure 1 shows how to solve the problem by adding a shift register.

For example, you can add an eight-LED bar graph to a design based on IC1, Freescale Semiconductor’s 9-bit, flash-memory MC68HC908QT1 microcontroller, which has only eight pins. The device includes only four general-purpose outputs and thus by default cannot drive eight discrete LEDs. To solve the problem, you can add IC2, a 74HC595 serial-input/serial-output/parallel-output latching shift register available from On Semiconductor and other vendors. The register’s latching function allows selective drive of only those LEDs associated with specific data bits.

According to its data sheet, the 74HC595 accepts signals through the SPI protocol. Unfortunately, low-end microcontrollers, such as the MC68HC908QT1, lack SPI hardware, but you can simulate the SPI in software by following these steps:

1. Unlatch the shift register’s outputs by deasserting microprocessor IC1’s PA4 pin.
2. Starting with the MSB, copy a bit from the processor’s internal data register and transfer the bit to the processor’s PA0 (SD) output.
3. Generate a clock pulse at Pin PA1.
4. Repeat steps 2 and 3 for all eight data bits.
5. Assert the microprocessor’s PA4 output to latch the data into IC2, the 74HC595.

Figure 2 shows the timing diagram for transmitting data byte $F0 from IC1 to IC2.

Available from the online version of this Design Idea at www.edn.com/050804di1, Listing 1 illuminates the LEDs by sending five consecutive bytes to IC1, and the LEDs: $03, $0c, $30, $c0, and $55. The first four bytes progressively illuminate two LEDs along the bar-graph display at one step per second. The last byte illuminates and latches all odd-numbered LEDs. The listing contains only commonly used instructions that easily translate into other microcontrollers’ assembly languages.

The SPI requires only three output pins, which frees the microcontroller’s remaining I/O pins for other functions and allows remote installation of the shift register/LED driver—for example, on a separate display board with the LEDs. Also, when suitably buffered, the register’s outputs can drive other loads, such as motors, relays, and incandescent lamps.

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Figure 1 Do you need more outputs? You can emulate an SPI in software to add a shift register to a pin-limited microcontroller.

Figure 2 The sample timing diagram illustrates the loading of $F0 byte into an external shift register.