In an eventually deadlocked state, the FSM moves from State 2 to State 0 until the count reaches a value of 4. The FSM then locks in State 2.

```verilog
module fsm(clk, rst_n, out);

input clk;
input rst_n;
output out;

reg out;
reg[1:0] cstate;
reg[3:0] cnt;

always @(posedge clk or negedge rst_n) begin
    if (~rst_n) begin
        cnt <= 0;
        cstate <= 'S0;
        out <= 0;
    end
    else case (cstate)
        'S0: begin
            out <= 1'b0;
            cstate <= 'S1;
        end
        'S1: begin
            out <= 1'b1;
            cnt <= cnt + 1;
            cstate <= 'S2;
        end
        'S2: begin
            if (cnt == 4'b0100)
                cstate <= 'S2;
            else
                cstate <= 'S0;
        end
    endcase
end
endmodule
```