<table>
<thead>
<tr>
<th>Verification method</th>
<th>Presilicon or postsilicon</th>
<th>Verification speed</th>
<th>Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate-level simulation</td>
<td>Presilicon</td>
<td>100 Hz</td>
<td>Slows with increasing complexity and number of gates</td>
</tr>
<tr>
<td>RTL simulation</td>
<td>Presilicon</td>
<td>10 kHz</td>
<td>Slows with increasing complexity and number of gates</td>
</tr>
<tr>
<td>ICE/hardware acceleration</td>
<td>Presilicon</td>
<td>500 kHz to 1 MHz</td>
<td>Constant speed</td>
</tr>
<tr>
<td>FPGA-based source-level emulation</td>
<td>Presilicon</td>
<td>more than 25 MHz</td>
<td>Constant speed</td>
</tr>
<tr>
<td>System validation</td>
<td>Postsilicon</td>
<td>Full clock (more than 400 MHz)</td>
<td>Constant speed</td>
</tr>
<tr>
<td>Compatibility validation</td>
<td>Postsilicon</td>
<td>Full clock (more than 400 MHz)</td>
<td>Constant speed</td>
</tr>
</tbody>
</table>