Motor uses simple reverse-battery protection

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This Design Idea presents a low-side, reverse-battery-protection technique for a dc-motor system. The system in Figure 1 incorporates two protection options. The common practice of using a diode for reverse-battery protection does not work with dc motors’ inductive loads. In Figure 1, an Allegro (www.allegromicro.com) A3940, a low-cost power MOSFET controller, drives a dc motor. An H-bridge for driving the motor comprises the n-channel MOSFETs Q0 to Q3. To change the motor’s direction from forward (current flowing from Phase A to Phase B) to reverse, the direction of current in the motor winding must reverse. This reversal means that Q0 and Q3 switch from on to off, and Q1 and Q2 switch from off to on. For an inductive load, the induced voltage, \( E = L \frac{di}{dt} \), where L is the inductance, and \( \frac{di}{dt} \) is the rate of change of the current. The induced voltage opposes any change in current. Therefore, after the switches attempt a current reversal, current continues to flow forward (forced by the induced voltage) from ground back to the power supply through Q0 and Q3. The current gradually decays to zero and then reverses direction. If a reverse-battery-protection diode is present in the current path, the decaying current is blocked and a large voltage can develop across the protection diode. Thus, the normal current recirculation meets interference. Further, the protection diode may break down, and potentially destructive voltages can appear on the FETs and the IC.

Figure 1 shows how to implement reverse-battery protection using the n-channel MOSFET, Q6, at the ground (low side) of a power supply. You can use either Option A (solid line) or Option B (broken line) to complete the circuit protection. If you use Option A, remove Q5. If you use Option B, you should cut open the bold trace marked “Option A.” In both options, Q6 is connected such that its source connects to the H bridge, its drain to the power-supply ground, and its gate to the VREG13 output (a regulated 13.5V). At power-up, the body diode of Q6, D1, is forward-biased and provides the dc current path that allows the IC to power up. As the VREG13 regulator powers up, it turns on Q6, which provides a lower resistance path to ground than does the body diode, D1. The current gradually decays to zero and then reverses direction. If a reverse-battery-protection diode is present in the current path, the decaying current is blocked and a large voltage can develop across the protection diode. Thus, the normal current recirculation meets interference. Further, the protection diode may break down, and potentially destructive voltages can appear on the FETs and the IC.

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not available and the Q₆ body diode, D₁, is reverse-biased, preventing any reverse-current flow.

We devised Option B because of a concern that switching noise may appear at the IC’s ground if Q₆’s on-resistance is not low enough. By opening the connection labeled Option A, you isolate the IC ground from the potentially noisier connection at the source of Q₆. Q₅ is configured and operates in the same fashion as Q₆. Q₅ can have higher on-resistance than Q₆, and, in this configuration, you may relax the on-resistance requirements for Q₆. Experiments have demonstrated that both options work equally well if you carefully choose Q₆’s on-resistance.

**Simple setup tests bit-error rate**

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Traditionally, the reception quality of a digital receiver is expressed in terms of BER (bit-error rate). This figure is the proportion of received bit errors in a given period. Typically, you measure the BER in the lab by applying an RF signal, modulated by a pseudorandom code, to the receiver under test. This Design Idea suggests an alternative method based on the use of a simple square wave. This method may not be superior to the usual technique, but it is simple to implement and gives a reliable result. The simplicity of the method is based on the fact that it requires no complex synchronization. Admittedly, a square wave is not truly representative of the data a receiver encounters in normal use (Figure 1). The square wave to modulate the RF carrier is phase-shifted to allow for the delay in the receiver. An exclusive-OR gate produces a sampling pulse at each bit transition—typically, 10% of the data-bit width. This sample pulse samples the raw data the receiver generates, producing clean data.

The key to understanding this technique is to keep in mind that a string of two successive ones or zeros indicates an error. A D flip-flop implementing a 1-bit delay detects the error.

You can display error pulses on an oscilloscope or count them by using a frequency counter. Figure 2 shows a typical test setup. You modulate the RF generator at the prescribed data rate. Note that a 500-Hz square wave is equivalent to a baud rate of 1 kbps. Both the modulating signal and the received data feed into the BER-test board. You adjust the sampling signal to be near the end of the received-data pulse. In many digital receivers, this arrangement yields a fair approximation to a correlation receiver. Error pulses appear on the oscilloscope. If you wish, for example, to set the RF level for a BER of 1-to-100, you reduce the RF level to the receiver such that, in a 100-msec sweep you see, on average, one error pulse per sweep.

In Figure 3, IC₁ and potentiometer P₁ form the basis of an adjustable phase shifter. R₁ provides hysteresis, and R₂, C₁, and IC₂ form a differentiator that provides a sampling pulse train. The first flip-flop clocked by the sampling pulse makes a hard decision concerning each bit. The next D flip-flop, together with exclusive-OR gate IC₂₃B detects the occurrence of two successive identical bits.
The simple BER tester uses an adjustable phase shifter and a differentiator.

This situation constitutes an error. A final D flip-flop and a transistor ensure that the Error output is clean. The construction of the system follows the circuit diagram in Figure 3. It sets an HP8647 RF signal generator at 868.35 MHz, and a function generator provides OOK (on/off-key) modulation. The receiver under test was a Melexis (www.melexis.com) TH7122 at 868.35 MHz in the OOK-modulation mode. Adjust the RF level to vary the error rate. This design obtains an RF level of $-107 \text{ dBm}$ for a 1-to-1000 BER and $-108 \text{ dBm}$ for a BER of 1-to-100, levels consistent with the data sheet. You should take care when you’re implementing OOK. Most RF generators provide AM. Thus, you must remove 3 dB from the displayed RF value. You can use this technique for other types of binary modulation, such as FSK (frequency-shift keying), for example.

Solar-powered motor runs on 10 nA

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Designs for solar-powered applications with low-duty-cycle requirements can often rely on capacitors for energy storage in place of less reliable batteries. Typical applications include solar positioning, telemetry transmitters, chemical pumps, data loggers, and solar-powered toys. The circuit in Figure 1 can run a small pager motor from the output of a small calculator-type solar cell in near darkness. The circuit works by repeatedly charging a 4700-μF capacitor, $C_1$, to 1.75V and then dumping the charge into the motor. Only the self-leakage current of the solar cell limits low-light operation. The circuit itself has such low leak-
Photovoltaic switch disables unused LEDs

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In many applications, it’s desirable to disable LEDs used for system verification. Many options are available for the disabling function, including manual SPST (single-pole single-throw) switches, enhancement- and depletion-mode MOSFETs, bipolar-junction transistors, and JFETs. The circuit in Figure 1 automatically disables the LEDs when a mechanical housing encloses the circuit card, thereby preventing you from accidentally leaving the LEDs on to waste power. The main switch portion of the circuit comprises an amplified photovoltaic cell (photodiode) and a small, n-channel MOSFET. The amplified photodiode signal provides drive to the MOSFET’s gate when enough light is available. Because the photodiode generates its own power from the available light, the amplified photodiode IC consumes only microwatts in a unity-gain configuration.

Originally, I considered using a series string of photodiodes to directly drive the MOSFET’s gate. However, the integrated OPT101 design provides reliable operation under a number of light conditions. If you adjust the gain of the amplifier, the circuit can function in both bright and dim applications. I use multiple MOSFETs for unique voltage ranges in which the LED would suffer damage from excessive reverse-bias voltages. This precaution is important in a design with multiple power-supply voltages. For instance, if you used only one MOSFET to control the LEDs in a design using 3.3 and 12V supplies, the reverse voltage across the 3.3V LED would be 8.7V when the switch is off. This reverse voltage exceeds the absolute maximum rating for many LEDs. If you need to control status LEDs using a microcontroller or some other logic-level device, add another MOSFET between the LED and the light-switch circuit. This configuration allows the light switch to act as a master on/off switch and the logic device to act as a secondary on/off control.

Figure 1

This circuit configuration turns off unneeded LEDs when it’s dark.
Assume that a design requires positive voltage, but only a negative-voltage power source is available. Using a standard boost-converter IC in the circuit of Figure 1, you can efficiently generate a positive voltage from a negative source. The boost converter generates an output voltage that's higher than the input voltage. Because the output voltage—5V in this example—is higher than the negative-input-voltage ground level, the circuit does not violate the boost-converter principle. The circuit in Figure 1 uses the EL7515, a standard boost converter. The ground pins of the converter IC connect to a negative-voltage input source. Ground becomes the "positive" input source. $V_{OUT}$ is as follows:

$$V_{OUT} = -V_{FB} \left( \frac{R_2}{R_1} \right) = -1.33V \quad (37.5\, \text{k} \Omega / 10k\, \Omega) = -5V.$$  

The $Q_1$ and $Q_2$ pnp transistors form a translator that scales the 5V output voltage (referred to ground) to a feedback voltage referred to the negative input. The transistor pair also eliminates temperature-change and voltage-drop effects. As the negative input voltage decreases, $Q_4$ runs at an increasingly higher current than $Q_3$, causing additional transistor-offset mismatch.

For optimal line regulation, you should set $Q_3$ and $Q_4$ to operate at the same currents with the nominal input-voltage applied. Figure 2 shows the line-regulation results. The maximum output-to-input voltage difference must be within the boost converter’s internal power FET drain-to-source breakdown voltage ($V_{DS}$). For the EL7515, the maximum $V_{DS}$ is 18V. For the 5V output, the minimum (most negative) input voltage is $-12V$. A 1V safety margin compensates for the $D_1$ diode drop and any voltage spikes on the drain of the power FET. Figure 3 shows the load-regulation test results. The maximum output current is a function of the input-to-output voltage ratio and current-limit setting of the boost converter. As Figure 4 shows, the circuit yields greater than 80% efficiency at 200-mA output.