SUCCESSFUL DESIGN OF HIGH-SPEED, HIGH-PIN-COUNT ICs
REQUIRES PACKAGING ENGINEERS AND CHIP DESIGNERS
TO WORK CLOSELY TOGETHER THROUGHOUT THE PROJECT.

When the package means as much as the chip

As high-speed data access, transmission, and storage move from high-end computing and long-haul SONET (synchronous-optical-network) applications into portable computing and Ethernet LANs (local-area networks), semiconductor devices need to grow more cost-effective while meeting increasingly stringent performance requirements. ICs for data transmission at speeds generally greater than 2.5 Gbps now range from data-multiplexing signal transmitters having fewer than 200 total signal, power, and ground connections to high-speed physical-layer fabric-switching devices that require more than 2000 connections. At both ends of the application spectrum, the electromagnetic properties of the substrate interconnecting circuits affect the overall product performance. The pursuit of the least expensive, smallest, most reliable packages magnifies these electromagnetic effects and increases the importance of design details.

Historically, semiconductor-component packaging for high-data-rate signal transmission took the form of small, low-pin-count LGAs (land-grid arrays) on low-loss ceramic substrates. Minimizing wire spans or replacing them with solder-bump interconnects minimized chip-to-package interconnect inductance. The use of ceramic substrates enables adequate spacing of the signal lines and corresponding reference planes using as many as 20 substrate layers. Organic substrates can include as many as 10 layers, but four to six are more typical. In the past, the dielectric properties and manufacturing process control of organic substrates were inadequate to reliably meet product-signal-integrity requirements, even at less than 1 Gbps. Now, various dielectrics are available for organic substrates (Figure 1). Process control also continues to improve, thereby enabling tighter spacing of 3-D interconnect structures. More significant, though, is the impact of increasingly sophisticated techniques for chip/package co-design, modeling, and simulation.

The combination of tighter process tolerances, more accurate material-property measurement, and more intelligent substrate design and simulation enable cost-effective organic packages to outperform far more expensive previous-generation units.

KEY ENGINEERING CHALLENGES

To improve performance, cost, and speed, manufacturers strive to design ICs into mainstream, high-volume, organic packages. Various substrate technologies can deliver the necessary performance; each has its own set of key challenges associated with addressing signal-integrity and cost issues. Factors that affect cost include unit volumes, body size, number of layers, critical dimensions, and manufacturing efficiency. Figure 2 shows how body size affects the relative price of four substrate technologies that permit high-frequency, high-performance designs. The substrate technologies include: BT (bismaleimide triazine)/wirebond—a four-layer, BT substrate with mechanically drilled vias; BT/flip-chip—a four-layer, all-BT substrate with blind or buried laser-drilled vias; thermal-setting epoxy/flip-chip—a build-up 3-2-3-layer structure comprising thermosetting-epoxy lay-

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**Figure 1**

**Figure 2**

Package-substrate high-frequency losses vary over a range of more than 20 to 1, and costs vary by approximately 50 to 1.
design feature Packaging high-speed ICs

ers on a BT core with blind or buried laser-drilled vias; and ceramic/flip-chip—an all-ceramic, 10-layer structure with punched vias. The substrate price increases with body size for all of these technologies, but the rate of increase varies because of factors that the preceding paragraph mentions. Figure 2 does not consider the effect of layer count on substrate cost.

The relative prices in Figure 2 are from actual designs and quotes obtained in multiple technologies. For a given design, the price is lower in the organic technologies, yet careful design can deliver performance comparable with that of ceramic substrates. The desire for an increasing number of I/O connections drives the need for larger body-size packages. As the number of bond pads increases beyond approximately 1000, area-array flip-chip technology most efficiently uses the chip area. When a design employs fewer pads, wire-bond approaches continue to be more cost effective. Each of these substrate technologies presents its own combination of challenges for high-speed designs and may require trading off performance for density. Achieving the best performing, most reliable, lowest cost design requires extensive and proven methodologies for IC/package co-design, package-simulation and -characterization, and product-performance verification.

Increases in the speed, density, and complexity of components for high-data-rate signal transmission have heightened the challenges that designers face in maintaining signal integrity through the IC/package interconnect and the package. The following discussion briefly addresses some of the key challenges in preserving 2.5- to 10-Gbps signal waveforms through densely routed packages. Important considerations include the effect of very dense designs on signal integrity (impedance matching, high frequency losses, and other factors) as well as the impact of such designs on power supplies.

Electromagnetic phenomena present design issues in signal routing for high-speed, high-frequency IC applications because, at the frequencies involved, the dimensions often represent substantial fractions of a wavelength. Transmission-line effects, high-frequency propagation losses, and EMI (electromagnetic interference) are some of the phenomena that affect signal integrity at these frequencies. You must consider both the clock frequency and the signal rise time to ensure signal integrity over the application’s entire bandwidth.

THE OLD DAYS ARE GONE

Historically, designing high-speed signals into small, low-pin-count packages required little attention to impedance matching. Compared with today’s signals, the rise times were long, and the effective signal paths were short. Often, designers used frequency-domain measurements to tune and build the packages to meet scattering-parameter targets. As current and future generations of high-speed devices move into larger and denser packages with longer effective signal paths that approach transmission-line structures, impedance matching becomes more important. During IC/package co-design, IC and package designers often agree on impedance targets and signal configurations—such as single-ended, differential pair, and coplanar—for routing signals between the die and the package pins. Because the methods of achieving impedance targets are rarely unique, package designers must choose IC- and package-interconnect schemes that optimize a number of substrate variables. These variables include the number of routing layers; stackup topology; variation of the dielectric properties with frequency; and the manufacturing variability of trace widths, spaces, and layer thickness.

Package designers must consider high-frequency losses as well as transmission-line effects. All aspects of 3-D topology affect high-speed signals’ behavior in the package’s complex environment. The initial characteristic-impedance match helps to reduce transmission-line reflections in each layer. Because physical discontinuities can contribute to multiple reflections, the design must minimize—or at least control—all of the discontinuities along the entire signal path. To ensure performance, both package and chip designers must understand the effects of factors such as wire bonds, flip-chip-escape routing, vias, trace bends, routing over holes in planes, stackup topology, and materials. Because their distributed nature strongly influences the rise time (or the bandwidth in the frequency domain), these package features require proper design and characterization based on rise time.

Transmission loss is another serious issue in high-speed IC-package designs. Two types of transmission losses exist: skin-effect losses and dielectric losses. Skin effect, which is proportional to the square root of frequency, leads to an increase in conductor dissipation. At high frequencies, significant skin-effect losses degrade signal-waveform amplitudes. In lossy materials within substrate layers, the dielectric constant’s frequency dependence leads to dielectric leakage at very high frequencies. Although simulation or measurement can quantify these losses, package designs should, whenever possible, use low-loss dielectric materials.

As a system’s switching speed increases,
es, electromagnetic radiation can produce troublesome EMI. Although EMI increases with crosstalk, the mechanisms of EMI and crosstalk differ greatly. Radiated emissions associated with multi-gigabit-per-second data rates can introduce noise via signal lines, power and ground planes, and traces. This noise can superimpose itself on signals as they travel between nets, between chips in a single system, and between systems. Also, predicting the radiation of complex structures, such as packages, is difficult. Avoiding EMI through careful planning is easier, less costly, and faster than trying to correct EMI-induced system misbehavior after you discover it.

Packages sizes have grown to accommodate an increasing number of high-speed signals (200 differential pair) and total I/O (2000 signals). In addition, IC and package interconnects have grown more dense employing tighter wire-bond pitches with longer wires (often double and triple rows of staggered pads) or finer bump pitches (including both peripheral and core-signal connections). Earlier discussions have covered the use of larger package bodies and the effect of the resulting increase in trace length. For wire-bonded packages, the decrease in effective wire pitch can lead to increased coupling or crosstalk, whereas the greater wire length can significantly increase the signal-path inductance. These factors directly conflict with high-speed-signal design rules.

Using flip-chip packages addresses some of these issues but creates different concerns. Although the bump inductance is significantly less than that of a wire, the very dense, complex routing of signals leaving the substrate’s die area can reintroduce inductance and cause reflective losses and vertical coupling. Signals can escape the congested bump-pad area through narrow traces that pass between the outer bumps. When you combine these narrow traces with the bump, pad, and via, the traces can exhibit parasitic inductance similar to that of wire bonds.

An alternative approach is to route some signals directly down through vias to the corresponding substrate-routing layer. This technique requires a series of stacked vias and presents the possibility of multiple discontinuities—and reflections—between each via in the stack. An increase in via density along with larger via diameter can lead to vertical or via coupling for which the design must account. Increased via density also causes an increase in the number of clearance holes in the package power and ground planes. The design must further account for impedance and parasitic changes to the planes and their effects on signal traces that pass over holes. Avoiding these hurdles in density causes package-body sizes and sometimes chip sizes to increase.

Die shrinks, increasing package density on pc boards, and larger numbers of signals switching simultaneously are making power distribution as important in the package and on the board as on the chip. The package’s power and ground networks must minimize IR drops and ground bounce. Some designs require split planes to support different IC power supplies. You must carefully design the split planes to minimize the resistance and inductance of all critical power and ground connections from the chip to the package plane as well as from the package to the board. Package-design verification through static and dynamic IR drops and SSN (simultaneous-switching-noise) analysis is becoming a necessary step in product design flow. More and more cases require adding decoupling capacitors to improve power and ground integrity, which these product simulations must include.

IC AND PACKAGE CO-DESIGN

During the last 12 months, the concept of IC and package co-design has grown significantly in popularity among semiconductor vendors. Increases in density, complexity, and operating frequencies impose additional constraints on both the IC and the package. The large number of constraints can easily lead to optimization of some parameters at the expense of others. The IC- and package-design methodologies need to merge, and designers must establish clear specific co-design milestones and reviews on the product-design calendar. Freezing a die’s pad and bump placements and substrate-ball maps represent critical milestones that accommodate current advanced-design-substrate-procurement intervals without adversely affecting product-delivery schedules.

During co-design, the design-team members translate the final IC and product requirements into interconnect- and package-performance targets. For ICs that incorporate several buses, which require various driver sizes, speeds, and supply voltages, determining the cell placement and pad/bump locations must go hand in hand with consideration of the package design. To allow parallel design of the IC and the package, chip and package designers must agree early in the project on substrate technology, layer stackup, critical-signal routing, treatment of differential pairs, and power-plane splits. A true co-design approach represents more than a combined flow or methodology; it constitutes a culture committed to making trade-offs to optimize the final packaged product’s cost and performance.

Early in IC- and package-co-design
projects, designers consider certain package parameters, such as characteristic impedance, time delay, and power-plane inductance. Accurately addressing other important signal-integrity metrics cannot proceed, however, until completion of the first design iteration and creation of a 3-D routing and stackup for at least the section of the package that contains the critical or high-speed signals. You can categorize these parameters in the frequency and the time domains. In the frequency domain, the key parameters for signals are return loss, insertion loss, and crosstalk, which you usually express as scattering parameters. For power and grounds, the keys are IR drops and inductance extractions. In the time domain, the keys for signals are ringback, overshoot, undershoot, delay, crosstalk, flight time, flight-time skew, jitter, BER (bit-error rate), and ISI (intersymbol interference). Because of simultaneous signal switching, a key for power and ground distribution is SSN. Package designs require proper characterization of both frequency- and time-domain effects to ensure the preservation of IC-signal integrity to the board.

To adequately characterize interconnect and package performance, Agere Systems uses a methodology that integrates electromagnetic simulation and package measurement. This methodology provides an equivalent measurement step for each simulation step (Figure 3). At any characterization stage, designers can compare and correlate results in either the frequency or the time domain. In the simulation approach, validated commercial tools extract parasitic parameters of complex package structures. Depending on the application, quasistatic or full-wave approaches can be necessary for the full package, particular sections, or just for critical nets. Furthermore, equivalent circuits extracted from the electromagnetic solutions enable subsequent circuit simulations, especially time-domain analyses.

The measurement approach usually involves the design of test fixtures. Separating fixture effects requires careful deembedding. A vector-network analyzer measures the scattering parameters of the device under test and the test fixtures and allows extraction of empirical circuit models from the initial test results. Time-domain reflectometers provide an alternative approach for empirical models.

Designers can compare both the simulation and the measured results with industry specifications and the characteristics of available packages. Calibration and correlation of all of the paths allows using any path or combination of paths to simulate product performance to minimize risk, cost, and design time.

The IC and package co-design translates the IC and product requirements into package targets. During the co-design, designers make high-level product trade-offs (high-speed performance versus signal density, for example) and define product architecture, pad/bump locations, and ball maps. During the package simulation and characterization, designers extract parasitic-element values and use them in system-level simulations to assess the package performance and compare it with the product targets.

Product- and system-level performance verification establishes the ultimate success of the IC and package-design and characterization methodologies. Simulation and testing of the final product (or packaged test die) demonstrates performance to customers and provides feedback to the co-design and characterization teams. The simulated and measured eye diagrams of Figure 4 provide examples. Figure 4a shows a simulation of a 3.125-Gbps serializer/deserializer signal from the IC through the package and through 40 cm of backplane. Figure 4b shows the corresponding measurement of the IC, package, and test board. Comparison of the figures shows a good level of agreement (predicted eye opening of 320 mV and measured eye opening of 326 mV).

The ability to merge IC and package simulation and characterization into a component or system simulation is critical to the final product’s success. In addition to providing customers with the ability to accurately simulate one or more products in the system, the capability also closes the loop on the end-to-end design flow. Once the designers establish and verify a product-simulation methodology, they can determine the effects of different IC and package approaches and make appropriate trade-offs—particularly for products that contain several high-speed signals. Finally, the design team can quantitatively establish the validity of the initial performance targets (impedance matching, return and insertion losses, noise, and timing budgets). This information enables continuous improvements in the co-design process as well as production of the lowest cost, best performing products.

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