Small, 915-MHz antenna beats monopole

Dave Cuthbert and Bob Casiano, Micron Technology, Boise, ID

A 915-MHz data-acquisition project required a small antenna, but the available antennas lacked the necessary characteristics: efficiency, compactness—that is, smaller than a standard 3-in. monopole—with adequate bandwidth, and with amenability to modeling by inexpensive NEC-2 antenna software. (To learn more about NEC antenna software, go to www.nitscientific.com/nec.) The result of this design effort, called the “Tab” antenna for its square shape, has the following characteristics:

- a square shape, 1.25 in. per side (0.1 wavelengths);
- the ability to be constructed in FR-4 pc board;
- linear polarization;
- a 2-to-1 VSWR (voltage-standing-wave-ratio) bandwidth of 46 MHz (5% bandwidth);
- the ability to be mounted parallel or perpendicular to a pc board;
- enhanced suppression of second- and third-harmonic radiation; and
- the ability to be mechanically trimmable to resonance.

The Tab antenna is a folded monopole that you miniaturize by forming it into an inverted L with a downward bend at the end (Figure 1). You can solder it perpendicular to a pc board or build it as part of a pc board and place it at a corner. The folded section transforms the 12.5Ω radiation resistance to 50Ω and provides second-harmonic suppression. Third-harmonic suppression comes from an open stub near the base of the antenna. Detailed NEC-2 modeling explores the sensitivity to changes in the dimensions and optimized harmonic suppression. Because NEC models wire antennas in a vacuum and the Tab antenna is built on FR-4, you must incorporate the dielectric properties of the dielectric between the antenna elements into the model.

To incorporate the dielectric properties, you add periodic RC loads between the transmission-line elements. The loads are the small boxes in Figure 2, and each load comprises a 30Ω resistor in series with a 78-fF capacitor. The capacitance of each RC load is equal to the difference between the transmission-line capacities calculated with FR-4 as the dielectric and with vacuum as the dielectric. You calculate the resistance of each RC load using the published FR-4 loss tangent of 0.02. The following formulas determine the approximate RC values for the transmission-line loads:

\[
Z_0 = \frac{276}{\sqrt{\varepsilon_r}} \log_{10} \left( \frac{2D}{d} \right),
\]

where D is the conductor spacing and d is the conductor diameter.

\[
C = \frac{t_{\text{PROP}_\text{VACUUM}} \sqrt{\varepsilon_r}}{Z_0}
\]

\[
R = \frac{\text{LOSS TANGENT}}{2\pi f C}.
\]
You calculate the RC load parameters for 915 MHz and place them every 0.1 in. (approximately 5°) along the line. You use the following parameters in the calculations:

- \( D = 62 \text{ mils} \)
- \( d = 20 \text{ mils} \)
- effective \( Er \) (dielectric constant) of FR-4 = 3,
- loss tangent = 0.02, and
- \( \tau_{\text{PROP\_VACUUM}} = 85 \text{ psec/in.} \)

Table 1 shows the effective parameters in air and in the FR-4 medium. You use iterative modeling to determine the antenna dimensions with the following design parameters: The first vertical section and the horizontal section must be of equal lengths, the feedpoint impedance target is 50\( \Omega \), and the resonant frequency is 915 MHz. You meet these design criteria with a simulated antenna height of 1.3 in. and a total element length of 3.3 in. The actual element length of 3 in. stems from dielectric loading. You also shorten the actual antenna height to 1.25 in. to compensate for the impedance increase that the dielectric loss causes. Note that the modified NEC model accounts only for the dielectric between the antenna elements.

### Table 1—Antenna Parameters in Air and in FR-4 PCB-Board Material

<table>
<thead>
<tr>
<th>Material</th>
<th>( Er )</th>
<th>( Z_0 (\Omega) )</th>
<th>( C (\text{fF}) )</th>
<th>( R )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air</td>
<td>1</td>
<td>219</td>
<td>39/0.1 in.</td>
<td>Infinite</td>
</tr>
<tr>
<td>FR-4</td>
<td>3</td>
<td>126</td>
<td>117/0.1 in.</td>
<td>30( \Omega )</td>
</tr>
<tr>
<td>RC load</td>
<td></td>
<td></td>
<td></td>
<td>78</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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The folded section, functioning as a shortened 180° transmission line at 1830 MHz, provides second-harmonic suppression. And, although the optimum point for the short circuit is 1.75 in. from the feedpoint, you can achieve second-harmonic suppression of 25 dB by placing the short within 10% of this point. The location of the short has little effect at 915 MHz. An open transmission line at the feedpoint that is 90° at 2745 MHz provides third-harmonic suppression. This line creates a near-short circuit at 2745 MHz and provides harmonic suppression of 15 dB when you trim it to within 5% of the optimum length. The large bandwidth of the Tab antenna results in low sensitivity to environmental detuning. This design effort yields an antenna only 40% as tall as a standard quarter-wavelength monopole, yet having excellent radiation efficiency, extended bandwidth, and superior harmonic suppression.

### Table 2—Harmonic Suppression of Quarter-Wavelength Monopole and Tab Antenna

<table>
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<th>Frequency (MHz)</th>
<th>Quarter-wavelength monopole (dB)</th>
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<tr>
<td>1830</td>
<td>7</td>
<td>25</td>
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<td>2745</td>
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The circuit of Figure 1 produces an accurate, variable-frequency sine wave for use as a general-purpose reference signal. It includes an eighth-order elliptic, switched-capacitor lowpass filter, IC\(_1\), which uses a 100-kHz square-wave clock signal that microcontroller IC\(_2\) generates. (Any other convenient square-wave source is also acceptable.) The microcontroller receives its clock signal from a 10-MHz oscillator module. A voltage supervisor, monopole with a 50\( \Omega \) source driving both antennas.

The Tab antenna has 20-mil-wide traces on opposite sides of 62-mil FR-4 and mounting pads at three locations to allow soldering the antenna securely to a larger board. You tune the antenna by trimming the open transmission line to provide an impedance minimum at 2745 MHz and then trimming the antenna elements to resonance at 915 MHz. Figure 3 shows that the simulated 2-to-1 VSWR bandwidth is 41 MHz, whereas the measured bandwidth is 46 MHz. Note that the required operating band is only 902 to 928 MHz. The increased measured bandwidth arises from dielectric losses and indicates that the radiation efficiency is approximately 90%. The large bandwidth of the Tab antenna results in low sensitivity to environmental detuning. This design effort yields an antenna only 40% as tall as a standard quarter-wavelength monopole, yet having excellent radiation efficiency, extended bandwidth, and superior harmonic suppression.

### Digital signal controls sine generator

Simon Bramble, Maxim Integrated Products, UK

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LISTING 1—ASSEMBLY CODE FOR SINE GENERATOR

When you connect remote sensors to a central process controller, a simple, robust, and commonly used interface is the 4- to 20-mA loop. The advantages of this current loop include the simplicity of just two twisted wires that share both power and signal, the loop’s high noise immunity in harsh environments, and the de facto loop standard within the process-control industry. Within this interface scheme, a typical 24V battery poses it on a dc level of \( V_{cc}/2 \). The result for a 5V input is a 2.25V peak-to-peak output. Listing 1 shows the assembly code for the microcontroller this application uses. You can download the code from the Web version of this Design Idea at www.edn.com.

Transmitter accurately transfers voltage input

Clayton Grantham, National Semiconductor, Tucson, AZ

This ideal 4- to 20-mA current transmitter has one voltage-controlled current source and one fixed current source.
Figure 2 allows you to transmit current (4 to 20-mA loop) with less than 1% total error from −40 to +85°C and over a 3.2 to 40 V loop-voltage range. Many IC realizations of a current transmitter have existed for years, but none operates at the loop voltage of 3.2 V. Also, these ICs are becoming sensor-specific, whereas you can modify and optimize the circuit in Figure 2 for any sensor electronics or loop-current variation (for example, a 1 to 5 A loop) at low loop voltage. The total loop current is as follows: Loop current = 1.225 V (R11/R10)/R3 + V\text{IN}/R2. The circuit discussion starts with the realization of the fixed current source, I_c. The fixed 4-mA current all flows through R_c. The servo circuitry, including IC_1 and IC_2, senses the 44-mV voltage drop across R_c and keeps it fixed. Note that the ground current of all ICs also flows through R_c; thus, the 4 mA fixed-current setting includes ground-current errors. The dual op amp, IC_3, is both an inverting gain stage and an integrator stage. R_d and R_e set the inverting gain to −27.8 V/V. The noninverting-integrator components C_3, C_2, and C_1, and R_d provide a comparison of the −44 mV across R_c (gained up to 1.225 V) to the shunt-reference voltage of IC_4. The output of IC_4 adjusts the sum of the current through R_d and any ground current from IC_3, IC_4, and IC_5 to a value of 4 mA. IC_5 acts as an analog power-on-reset circuit that holds off the start-up of servo action until all the ICs have sufficient supply voltage. With the divider ratio of R_d and R_e and the 2.32 V option of IC_4, the start-up voltage equates to: V_{START-UP} = 2.32 V (R_3 + R_9)/R_9 = 2.7 V.

This start-up value is higher than the rated supplies of IC_1 and IC_2 and lower than IC_3’s regulated output of 3 V. R_c, level-shifts the output of IC_2A up from zero. R_c biases IC_2 into its specification range to guarantee 0.1% tolerance and 50 ppm/°C temperature coefficient over the −40 to +85°C range. The circuit discussion continues with the realization of the voltage-controlled current-source. IC_4, Q_1, and R_1 are configured as a voltage-to-current converter. Thus, for a full-scale range of 20 mA, 16 mA comes from the voltage-to-current converter. With the maximum V_{IN} at 1.2 V, R_2 must be 75 ohms to produce 16 mA. IC_4 must have a common-mode input range that goes beyond its negative supply (less than −44 mV). R_c is optional and prevents an open circuit on IC_3’s input. You can remove R_c, depending on the output impedance of any input-sensor electronics. Note that R_c directly introduces an error in the full-scale loop current.

At the heart of the circuit discussion is the realization of an output impedance, R_{OUT}, greater than 20 MΩ in Figure 1. The low-dropout regulator, IC_5, accomplishes this task by subregulating the supply to IC_4 and IC_5. The good line regulation of IC_5 keeps the 3 V output within 30 mV over the input range of 3.2 to 40 V. Additionally, IC_5 requires as little as 200 mV of overhead to properly regulate, and it
can withstand more than 40V. This current-transmitter circuit is useful for both low-loop-voltage designs, and it’s back-ward-compatible with higher loop-voltage implementations. Furthermore, IC₃ has reverse-supply and surge protection. Therefore, this circuit does not require an additional diode within the loop, a common need with other ICs to prevent accidental reverse-wiring damage. The TO-252-package option simplifies the thermal-design considerations. With a 1-in.-sq-area pad for heat sinking, the worst-case power dissipation calculation would keep the junction temperature within its rated 150°C: Tⱼ=85°C+(20 mA)(40V)×50°C/W=125°C.

You could increase the Vᵃᵣ range of the current-transmitter by scaling R₃ as long as you don’t violate the common-mode input range of IC₂. IC₂’s Vᵃᵣᵢ includes its positive rail. So, to obtain a higher Vᵃᵣᵢ, you can increase the voltage option of IC₂. For example, use the LM2936-5V and R₂ equal to 312.5Ω for a 0 to 5V input range. This configuration would also require that the loop supply be at least 5.2V. Note that any sensor and other electronics can and should use the 3V subrails that IC₂ creates as long as the current they demand does not exceed 3mA. The 4-mA fixed-current circuitry adjusts for the current demand. Figure 3 shows the total error on prototype units over temperature.

The total error includes the offset (4-mA) and full-scale (20-mA) effects on the ideal loop current. The tolerances of R₃, R₄, R₅, and R₆ should be within 0.1% with 50-ppm/°C temperature coefficients. With IC₃ sub-regulating the rails of IC₁, IC₂, and IC₃, the power-supply-rejection-ratio error of these ICs does not generate a significant error. In like manner, IC₃’s CMRR (common-mode-rejection-ratio) error does not generate a significant error. IC₃’s CMRR error and Q₁’s base-current error both influence the best nonlinearity attainable: less than 0.01%. IC₃’s offset error is in series with the 44-mV voltage across R₃, producing an offset error of 4mA. Adjust R₅ if you need to null this error. Adjust R₄ to fine-tune the full-scale range of 20mA. The op amp’s offset-temperature-coefficient error is small compared with the ±1% temperature-range budget.

### Absolute-value circuit delivers high bandwidth

Ron Mancini, Texas Instruments, Bushnell, FL

Most absolute-value circuits have limited bandwidth and high component count, and they require several matched resistors. The circuit in Figure 1 uses three fewer components than most absolute-value circuits require, and only two of the resistors must have 1% tolerance to obtain 1% accuracy. This circuit’s output voltage is an accurate representation of the absolute value of the input signal, and it is accurate for input signals containing frequencies as high as 10 MHz. Another advantage of this circuit is that it has a positive-voltage output, thus saving an analog inverter in most applications. When the input voltage is positive, the negative output voltage of IC₁ cuts off the diode, thereby preventing signal propagation through IC₁. Virtually no signal propagates through R₃, because the resistor connects to ac ground through the output of IC₂. The only signal path is through R₂ to buffer IC₂, and the output of the buffer is a positive voltage. When the input voltage is negative, the positive output voltage of IC₁ forward-biases the diode, thus providing an ac short circuit for R₁ to ground. IC₁ is within IC₂’s feedback loop, so the output voltage is positive because of IC₂’s configuration as an inverting op amp.

This design uses a dual op amp to minimize parts count. Two op amps in a feedback loop tend to be unstable. Select an op amp that has sufficient phase margin to prevent oscillation when the input voltage is negative. The circuit’s dynamic range is from the op amp’s input offset voltage to the maximum output voltage. This dynamic range is from 1 mV to 4.1V for the TLC072 with ±5V power supplies. The excellent bandwidth performance results from combining the high-frequency TLC072 op amp with a fast Schottky-barrier diode. You can use higher frequency op amps to obtain better bandwidth results, but you must take care in the op-amp selection to avoid oscillation or reduced dynamic range.

![Figure 1](https://www.edn.com)

This inexpensive absolute-value circuit has high bandwidth.

![Figure 3](https://www.edn.com)

On three prototype circuits of Figure 2, the total error is well below 1% over temperature at 3.2V loop voltage.