Simple circuit provides motor-feed control
Jean-Bernard Guiot, DCS AG, Allschwil, Switzerland

Because we needed a small grinding machine, we modified an old milling machine that lacked a control system. The table of the grinding machine needed only to move back and forth with adjustable feed. Using an existing dc servoamplifier, a servo motor, and limit switches, we devised the circuit shown in Figure 1. Because the motor had no tachometer, we used part of the motor voltage as feedback. We reduced the feedback voltage from the motor to approximately 8V by using the resistors R₁ to R₃. (Motor voltage = 60V, maximum amplifier input = 10V, R₁ = 33 kΩ, and R₃ = 10 kΩ.) This feedback voltage feeds back to the speed-command differential-voltage input. You must be careful with the feedback-signal polarity to avoid an uncontrollable runaway of the motor. The actual command voltage connects to the tachometer input, which is not differential. Using the appropriate gain and control-loop adjustments available on most drivers, you can obtain good motor response. This design uses the ±15V the driver supplies to power the control circuit. Switch S₁ enables manual and automatic modes. For both modes, potentiometer P₁ reduces the control voltage, and C₁ filters it. Two LEDs, D₁ and D₂, show in which direction the axis moves. This indication can be especially useful in automatic mode if the potentiometer is turned to its zero position. The driver becomes disabled in one direction when the inputs + Limit or − Limit no longer connect to 15V; that is, when the limit switch LS+ or LS− (located at each end of travel) become activated. The following describes the operation of the two modes:

- In manual mode, the momentary switch S₂ selects 15V or −15V. If you use two separate switches, take care to avoid shorting both power supplies together.
- In automatic mode, the polarity of the voltage depends on the setting of relay K₁. Upon power-up, K₁ is off; thus, a positive voltage goes to the driver. The motor moves in the positive direction until limit switch LS+ activates. At that instant, the driver is disabled (for the positive direction), and the relay, K₁, energizes. K₁ holds itself on through its

A defunct milling machine served as the platform for this grinding-machine motor controller.
In low-power, single-supply analog applications, it is often desirable to maintain precise control of voltages much greater than the positive-supply rail. The circuit in Figure 1 allows you to amplify the input voltage, \(V_{\text{IN}}\), by a factor, \(A\), which resistors \(R_1\) and \(R_2\) set. The output voltage, \(V_{\text{OUT}}\), equals \(A \times V_{\text{IN}}\), where \(A = \frac{R_2}{R_1 + R_2}\). The op amp receives its supply from a single 5V source, and the discrete output stage operates from a rectified voltage, \(V_s\), from a power source that meets the requirements of the application. When the circuit neither sinks nor sources current, the op amp’s output settles to a voltage higher than 1.9V (\(Q_1\) is completely off) but lower than the threshold voltage of the n-channel FET, \(Q_3\), minus 1.2V (two diode drops). When \(V_{\text{IN}}\) rises from a given state, the op amp’s output voltage drops and gradually turns on \(Q_1\). This action results in a voltage drop across \(R_8\), turning on \(Q_2\). This process continues until the voltages at the op amp’s two inputs match. A decreasing \(V_{\text{IN}}\) causes the op amp’s output voltage to rise to the point at which \(Q_1\) conducts enough to pull down \(V_{\text{OUT}}\). Capacitors \(C_1\), \(C_2\), and \(C_3\) are necessary to prevent oscillation.

The circuit, useful as a power driver for pulse generators, offers rise and fall times of less than 15 μsec, virtually independently of the supply voltage, \(V_s\). You can test the design with op amps LMC7101, LT1013, and AD8551. All these op amps deliver load currents as high as 5A at voltages as high as \(V_s = 40\text{V}\). One important feature of the design is its insensitivity to component tolerances. The values for \(R_5\) and \(R_6\) in Figure 1 yield \(A = 8\). The value of \(R_6\) depends on \(V_s\). You can then omit the components \(D_1\), \(D_2\), \(D_3\), \(R_4\), \(R_5\), and \(C_4\). In this case, the op amp’s output connects directly to the gate of \(Q_3\), and you must reduce the value of \(R_6\) to lower the base voltage of \(Q_3\) to maintain the “idle window” in which both \(Q_1\) and \(Q_3\) are off. The op amp’s input-voltage range must include ground. \(D_4\) is necessary only in cases in which sources connect to the output. \(D_4\) prevents reverse current flow from the external source through \(Q_3\). Such a situation can arise when the circuit serves in a battery-charger application.

The circuit in Figure 1 performs active voltage-to-current conversion or acts as a variable-gain current mirror with high precision and bandwidth. A typical application is testing high-speed ICs or other devices that have inputs designed to be driven from current-steering DACs to enable a modulated voltage source to control the devices. The circuit thus simplifies the testing of such devices in isolation, because modulated voltage sources are readily available, but modulated current sources generally are not. A further use of the circuit could be for easy and precise control of a current-controlled, variable-gain amplifier by using an adjustable dc voltage source at the input. Figure 1 shows the circuit configured as a voltage-to-current converter. The overall “gain” with the component values shown is 1 mA/V, but you can easily realize other gains by altering the component values. Note that the output of the circuit can both source and sink current.

Starting at the input, $V_{IN}$, because the input of amplifier IC$_1$ is at virtual ground, the parallel combination of $R_1$ and $R_2$ provides a 50Ω termination for the input signal. IC$_1$ then inverts this signal with a gain of $R_3/R_2$. Amplifier IC$_2$ provides a gain of $R_5/R_4$ to the signal received from IC$_1$, but its noninverting input is tied to the 3V reference. Therefore, its output and the top of the current-sense resistor, $R_s$, is offset by 6V with respect to ground when $V_{IN}$ is zero. The current source comprises amplifier IC$_3$ and the p-channel JFET, Q$_1$. The choice of a JFET, rather than a bipolar transistor, ensures very high speed, zero dc error, and almost perfect linearity in the output-current characteristic. The JFET is an SST175 from Vishay/Siliconix (www.vishay.com); it has a guaranteed I$_{DSS}$ current of 7 mA, high speed, and low

**Figure 1**

This versatile circuit can serve either as a voltage-to-current converter or as a variable-gain current mirror.
capacitance. Amplifier IC4 clamps the voltage at the source of Q1 and the bottom of R6 at 3V. With no signal input, therefore, Q1 passes a constant quiescent bias current of 3 mA into the 3-mA constant-current sink involving IC1 and Q2. The output current of the circuit, which comes from the drains of Q1 and Q2, is zero. When VIN assumes a level ΔV_{IN} above ground, the voltage at the top of R6 increases by the same amount. So the current through R6 and, thus, the output current, I_{OUT}, increases by an amount ΔV_{IN}/R6, equivalent to 1 mA/V.

This circuit differs from the traditional precision current-source topology (Figure 2) in that, the op amp in Figure 1 clamps the bottom end of the sense resistor at a constant voltage rather than being varied in response to the input signal. Instead, the voltage at the top end, which would normally be connected to a fixed voltage, varies in response to the input signal. Furthermore, because Q1 is always conducting, its gate-voltage variations are typically less than 200 mV in response to changes in VIN. The result is that no nasty current spikes transfer to the output via Q1’s gate-channel capacitance when VIN makes a step to or from zero. In a traditional circuit, because there is no current sink, the op amp must completely turn off the FET when the output current must be zero. In doing so, the op amp’s output slews several volts to saturation near its positive supply rail, transferring a high-amplitude current spike onto the output. A spike of the opposite polarity and similar magnitude is created when the op amp has to recover from saturation and slew in the opposite direction to again turn on the FET.

The 3-mA constant-current sink comprises amplifier IC1 and n-channel MOSFET Q1. IC1 clamps the voltage at the top of current-sense resistor R6 at −3V. Because the voltage-reference circuit fixes the bottom of R6 at −6V, the quiescent current through Q2 remains steady at 3 mA, equal to the current through Q1 when VIN is zero. When VIN assumes a level ΔV_{IN} below ground, the voltage at the top of R6 decreases by the same amount; the current through Q1 then falls below 3 mA; and the current sink obtains the balance of its current, ΔV_{IN}/R6, from the load.

The −6V reference that fixes the bottom of R6 derives from amplifier IC1’s applying a nominal gain of −2 to the 3V reference. You should trim the −6V reference by means of R_{14}, such that the output current is zero in the absence of an input signal; the quiescent currents in Q1 and Q2 are then equal. Note that this single adjustment entirely calibrates the signal path, canceling out the effects of resistor tolerance, amplifier dc errors, and any tolerance in the ±3V references but not the effects of finite open-loop gain. To ensure maximum bandwidth in the signal path, the amplifiers are AD8055-ARs from Analog Devices (www.analog.com). These amplifiers can tolerate a total supply voltage of only 10V, so you must operate IC1 from a split ±5V supply and IC2 and IC3 from a single-ended 10V supply, because their inputs are 3V above ground.

You can obtain optimum dc accuracy and stability by using an OP177GS amplifier for IC1 and IC2 and a high-quality reference IC, such as the AD780BR, for generating the 3V reference. You generate the −3V reference by applying a fixed gain of −1 to the 3V, using an inverting circuit similar to that used in Figure 1 for deriving the −6V reference. You should use 0.1% tolerance resistors where shown, and you can optionally include R_{12} to provide 0.11% of additional gain to compensate for the finite open-loop gain of amplifiers IC1 and IC2. You can further optimize the dc stability by including R_{15} and R_{16}, although the prototype does not use these resistors. In tests, without Cp the bandwidth of the circuit with a 1V peak-to-peak sinusoidal input was 80 MHz when the circuit drove a resistive 100Ω load. The output rise and fall times with the same load and a 1V, 2.5-nsec input step are just 5.5 and 4.8 nsec, respectively, with no overshoot, as measured with a 500-MHz oscilloscope. The typical output compliance ranged from 1.7V to −2.8V. The maximum undistorted output-current swing extended from +2.1 to −2.1 mA.

For optimum frequency response and linearity, you should use the circuit to drive a virtual-ground load; in other words, you should use a high-bandwidth op amp configured as a current-to-voltage converter. If you use any other load, which must have low impedance in any case, and it is partly capacitive, you may need a small capacitor, Cp across R6 to optimize the overall transient response of the circuit at the expense of some speed. You can also configure the circuit to operate as a current-to-current converter with an overall gain of 0.1 mA/mA by omitting R6, replacing R6 and R_{14}, with 0Ω, and increasing the value of R_{12} to 470 kΩ. You can use this configuration, for example, to scale the outputs from commercial current-steering DACs that typically have full-scale outputs in excess of those that ASIC inputs need. Thus, you could test an ASIC with current-driven inputs by using such a circuit between each input and each DAC output. Note that, in this configuration, amplifier IC1 is configured as a current-to-voltage converter with a gain of 0.1V/mA and presents a virtual-ground to the DAC outputs, a load that normally ensures optimum linearity performance from the DACs. The circuit supports both current-sourcing and current-sinking DACs, because the circuit can source as well as sink current. For high-speed operation, you may need a small capacitor across R6 to cancel the effect of the DAC’s output capacitance and any stray capacitance.

Chip recorder customizes phone ringer

Don Schelle and Ted Salazar, Maxim Integrated Products, Sunnyvale, CA

Companies usually purchase one type of telephone for all employees, which is understandable, especially if they obtain a discount for buying in quantity. One ringer sound for everyone can pose a problem, though, if the sound of a ringing phone makes a dozen people pause and look at their telephones. Equally annoying is the absence of a visual message indicator. Obliging everyone who suspects they may have a message to lift the handset and listen for a special message tone is far from ideal. By placing a circuit in series with the telephone, you can customize a phone ringer without modifying the phone (Figure 1). The heart of the ringer is a chip-recorder IC, IC5, which can play as much as 10 seconds of telephone-quality recorded sound.

This circuit plays as much as 10 seconds of recorded sound in place of the ring from a telephone. It also indicates when someone has called.
A high-efficiency stepdown converter, IC1, allows the circuitry to operate from a supply voltage of 5 to 14V.

An optocoupler and associated front-end circuitry monitor the line, sensing when the line receives a high-voltage ringer signal (Figure 2). Zener diodes D1 and D2 prevent the on-hook voltage from activating the optocoupler. Comparator IC3 latches LED D3 on when a call is received, and a pushbutton switch, S1, clears the comparator. The circuit shown in Figure 3 records as much as 10 seconds of sound in the chip recorder’s proprietary multilevel EEPROM. A switch-mode, Class D audio amplifier, IC6, maintains high efficiency and delivers adequate power to an 8Ω speaker; even a PC speaker will work.


Op amp linearizes attenuator control response
Mike Irwin, Shawville, PQ, Canada

Professional-audio equipment commonly uses Analog Devices’ (www.analog.com) high-performance, quad-voltage-controlled SSM2164 attenuator. The control response is $-30 \text{ dB/V}$, with 0V producing unity gain. Attenuation increases as the applied control voltage increases in the positive direction. The circuit in Figure 1 extends the range of applications for this versatile chip by providing a simple means of linearizing the control response. The result is an amplifier with gain directly proportional to the control voltage. In addition, the circuit also functions as a simple logarithm generator. You can use a single SSM2164 to make two high-quality, linear voltage-controlled amplifiers using this method. The four gain cells in the SSM2164 are tightly matched, current-in, current-out transconductance multipliers. The control response of each gain cell is: $\text{gain} = 10^{\left(-\frac{\text{VOUT}}{0.67}\right)}$. The cells are noninverting structures.

You can obtain both a gain-controlled output and a logarithmic output using this configuration.

Each voltage-controlled amplifier uses two gain cells. A “master” cell in the feedback loop of an op amp generates a logarithmic voltage output in response to a linear voltage input. This log voltage then goes to the control pin of the second
“slave” cell, which processes the audio signal. Op amp IC1 maintains its inverting input at virtual ground by servo-controlling the gain of the master SSM2164 cell, which connects to the negative reference voltage. The output of IC1 is a logarithmic function of the input: $V_{OUT} = -0.67 \log\left(\frac{-V_{IN}R_2}{V_{REF}R_1}\right)$. $V_{IN}$ is the gain-control voltage, and $V_{REF}$ is the negative reference voltage. $V_{OUT}$ then drives the control pin of the slave cell. Substituting the expression for $V_{OUT}$ for $V$ in the expression for gain yields the following: $\text{gain} = \left(\frac{V_{IN}R_2}{V_{REF}R_1}\right)$, which is the desired linear response.

Op amp IC2 converts the slave cell’s output current to an audio voltage with a gain of $R_4/R_3$. The overall expression for the gain is: $\text{gain} = \left(\frac{V_{IN}R_2R_4}{V_{REF}R_1R_3}\right)$. If $R_1 = R_2$ and $R_3 = R_4$, the expression reduces to: $\text{gain} = \frac{V_{IN}}{V_{REF}}$, and gain (in decibels) $= 20 \log\left(\frac{V_{IN}}{V_{REF}}\right)$. Setting $V_{IN}$ to 15V and $V_{REF}$ to −15V produces unity gain with the indicated component values. The gain decreases smoothly to $-70$ to $-80$ dB as the control voltage decreases (Figure 2). The voltage-controlled amplifier then shuts off completely (attenuation $= 100$ dB) when the control voltage drops to within a few millivolts of 0V. Negative voltages make the output of IC1 swing close to the positive rail, but IC1 promptly comes off the rail when the control voltage returns to the 0 to 15V range. The circuit produces no audible clicks and works well at lower supply voltages, such as ±5V.

For best performance, IC1 should be a low-offset, low-input-current unit, and IC2 should be a high-quality, low-noise audio op amp. However, you can obtain reasonably good performance with inexpensive op amps, such as the TL072 and LF353. The prototype unit achieved a control range of 75 to 80 dB, using an OP-290 for IC1. The control-voltage feedthrough on the audio output is minimal, varying 10 to 20 mV when you sweep the gain through a 70-dB range. The noise and distortion performance is excellent, because the design uses the gain cells in the standard configuration in the SSM2164 data sheet.