Some microcontroller applications usually use too many I/O pins to read keys or onboard switches; in many cases, few pins remain available for other uses. Some alternative ways to read keys yield more free pins. First, consider some ways to effect key reading. Table 1 presents a comparison of four methods with references to circuit configurations (figures 1, 2, 3, and 4). As you can see, the best choice for reading many keys is to use the A/D converter that is inherent in many microcontrollers. This option needs many lines of code and is not amenable to resistive buttons, such as flexible key pads (Reference 1). Another option is to read one key with one I/O port, but it needs as many pins as the keys to read.

Table 1—Various Key-reading Schemes

<table>
<thead>
<tr>
<th>Figure</th>
<th>No. of keys</th>
<th>No. of pins</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N</td>
<td>N</td>
<td>16 pins=16 keys</td>
</tr>
<tr>
<td>2</td>
<td>N</td>
<td>N/8</td>
<td>With ADC, 16 keys=two pins</td>
</tr>
<tr>
<td>3</td>
<td>N_XN</td>
<td>NIN+NOUT</td>
<td>16 keys=eight pins (four inputs and four outputs)</td>
</tr>
<tr>
<td>4</td>
<td>N</td>
<td>N</td>
<td>16 keys=five pins (four more keys available)</td>
</tr>
</tbody>
</table>

In this simple configuration, you need as many I/O pins as you have keys.

Using the microcontroller’s internal ADC, you need only two I/O pins to control 16 keys.
In a matrix configuration, you need eight I/O pins to control 16 keys.

With an expansion of this scheme, five I/O lines control 16 keys with room to add four more keys.
can add it for a real application. The program shows the variable KeyVal on three LEDs. You can probably write more efficient code that that of Listing 1; the code shown is just for testing. Table 1 shows how many pins you need to read 16 keys. As you can see, with the circuit in Figure 4, you need only five pins, but you can add four more keys. You can download Listing 1 from the Web version of this Design Idea at www.edn.com.

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PORT1</td>
<td>Input</td>
</tr>
<tr>
<td>PORT2</td>
<td>Output</td>
</tr>
<tr>
<td>PORT3</td>
<td>Input</td>
</tr>
<tr>
<td>PORT4</td>
<td>Output</td>
</tr>
</tbody>
</table>

Table 1 shows how many pins you need to read 16 keys.

Reference


LISTING 1—PROGRAM TO READ SIX KEYS AND DISPLAY RESULTS ON SIX LEDs

```c
#define KeyPin 0
#define KeyVal (KeyPin/4)

void MainProgram()
{
    KeyPin = 0;
    KeyVal = 0;
    while (1)
    {
        KeyPin = P0;
        KeyVal = (KeyPin/4);
        P1 = KeyVal;
    }
}
```

Synchronous buck circuit produces negative voltage

John Betten, Texas Instruments, Dallas, TX

Many electronic systems require both positive and negative voltages to operate properly. Generating an efficient, low-voltage positive output from a higher voltage input typically entails the use of a synchronous buck regulator. But when generating a negative output voltage from a positive input voltage, you’d typically use a flyback topology, especially at higher output currents. The operation and control characteristics of a synchronous buck and a negative flyback (also called a buck-boost) differ significantly. Figure 1 shows the basic components that a negative flyback circuit requires. When FET Q, turns on, the input voltage appears across inductor L, with no input current going to the load at this point. All the output current delivered to the load at this time comes from output capacitor C, because diode D, is reverse-biased. The current in the inductor continues building until the control circuit determines the proper time to switch off FET Q, At that point, the voltage polarity across inductor L, reverses in an attempt to maintain current flow, pulling the top side of the inductor to reverse.

**Figure 1**

This flyback topology produces negative output voltage from positive inputs.
negative with respect to ground and forcing diode D₁ to conduct. The output voltage goes negative to within a diode drop of the inductor voltage.

The duty cycle at which the control circuit operates also differs from that of a synchronous buck. Although the operating duty cycle of a synchronous buck is \( D = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \), the negative flyback operates at \( D = \frac{V_{\text{OUT}}}{V_{\text{IN}} - V_{\text{OUT}}} \). For example, if the desired output voltage is half the input voltage, the synchronous buck runs at 50% duty cycle, whereas the negative flyback runs at 33% duty cycle. The comparisons between the simple negative flyback circuit of Figure 1 and the synchronous-buck-controller negative flyback circuit in Figure 2 are straightforward. In Figure 2, FET Q₂ mirrors the function of diode D₁ in Figure 1 but with a decrease in the forward drop that occurs in the diode. This lower drop significantly improves efficiency. Diode D₃ conducts during the small dead time, when both FETs Q₁ and Q₂ are off, further reducing losses. The feedback voltage appears at the output ground through resistor R₁, because the control circuit is referenced to the negative output voltage. R₂ typically sets the output voltage to the desired level, because it does not change the feedback compensation network, as changing R₁ would. Desired changes to the input voltage, the output voltage, or both may necessitate an inductor-value change. The minimum inductor value is:

\[
L_{\text{MIN}} = \frac{\left| V_{\text{OUT}} \right| \left( V_{\text{INMAX}} \right)^2}{2f_{\text{MIN}} \left| \text{OUTMIN} \right| \left( \left| V_{\text{OUT}} \right| + V_{\text{INMAX}} \right)}.
\]

Take note of certain limitations with using the controller in this type of implementation. Because the control circuit is referenced to the negative output-voltage rail, the controller must have an input-voltage rating greater than \( V_{\text{IN}} + |V_{\text{OUT}}| \). The controller must also be rated for \( V_{\text{IN}} \) (minimum), which occurs at system power-up when the output voltage is zero. A controller that operates over a wide input-voltage range typically works best. The FET’s drain-to-source rating must also withstand \( V_{\text{IN}} + |V_{\text{OUT}}| \), and the FET carries peak currents that are greater than twice the output current. Low-resistance, fast-switching FETs produce the lowest losses. High efficiency is the major advantage of this circuit. Because the circuit uses n-channel FETs, as opposed to higher resistance and costlier p-channel parts, the circuit achieves peak efficiencies greater than 90%.

In developing electronic systems, designers look for products or ideas that may benefit from the better performance, smaller size, lower cost, and improved reliability that an IC can offer. Toward that end, the digital potentiometer emerged as an alternative to its mechanical counterpart, the mechanical potentiometer. The digital potentiometer offers most of the cited advantages but falls short for users of mechanical potentiometers, who require a simple rotary interface for front-panel adjustment or calibration without external controllers. The circuit in Figure 1 represents an attempt to combine the best of both worlds: the simplicity of a rotary interface and the performance of a digital potentiometer. The rotary encoder in this circuit is the RE11CT-V1Y12-EF2CS from Switch Channel (www.switchchannel.com). This type of rotary encoder has one ground terminal, C, and two out-of-phase signals, A and B (Figure 2). When the rotary encoder turns clockwise, B leads A (Figure 2a), and, when it turns counterclockwise, A leads B (Figure 2b).

Signals A and B of the rotary encoder pass through a quadrature decoder (LS7084 from LSI Computer Systems, www.lsisci.com), which translates the phase difference between A and B of the rotary encoder into a compatible output, CLK and U/D, that the AD5220 can accept. The AD5220 from Analog Devices (www.analog.com) is a 128-step, pushbutton digital potentiometer. It operates with a negative-edge-triggered clock, CLK, and an increment/decrement direction signal, U/D. When B leads A (clockwise), the quadrature decoder provides the AD5220 with a logic-high U/D. When A leads B (counterclockwise), the quadrature decoder provides the AD5220 with a logic-low U/D. The quadrature decoder also produces a clock in synchronism with its output, which also connects directly to the AD5220. You linearly vary the clock’s pulse width by adjusting R Bias.

Aside from decoding the quadrature output of the rotary encoder and providing a clock signal, the LS7084 also filters noise, jitter, and other transient effects. This feature is important for this type of application. Unlike optical encoders, the RE11CT-V1Y12-EF2CS is a low-cost electrical encoder, in which each turn can create some bounce or noise issues because of the imperfect nature of the metal contacts within the switch. The LS7084 prevents such erroneous signals from reaching the AD5220. The operation of the circuit in Figure 1 is simple. When the rotary encoder turns clockwise, the resistance from the wiper to terminal B1 of the digital potentiometer, RBW1, increments until the device reaches full scale. Any further turning of the knob in the same direction has no effect on the resistance.

Likewise, a counterclockwise turn of the knob reduces RBW1, until it reaches the zero scale, and any further turning of the knob in the same direction has no effect. One example of the flexibility and performance this circuit offers becomes apparent when you consider systems with front-panel rotary adjustment. You can lay out the compact digital potentiometer and quad-

**Figure 1**

A quadrature decoder and a digital potentiometer form a simple rotary-encoder interface.

**Figure 2**

In clockwise rotation, signal B leads A (a); in counterclockwise rotation, A leads B (b).
Amplifiers perform precision divide-by-2 circuit
Glen Brisebois and Jon Munson, Linear Technology Corp, Milpitas, CA

The classic implementation of a voltage-halving circuit uses two equal-value resistors. Using 1% resistors provides a divider output with 2% accuracy. For most applications, this performance is cost-effective and more than adequate. However, when you need extreme precision, this approach requires correspondingly accurate resistors and can become expensive. Putting feedback around a finite-gain instrumentation amplifier yields a divide-by-2 circuit with the added benefit of a buffered output. The operation of the circuit is straightforward. The instrumentation amplifier has unity gain, so the voltage it sees across its inputs appears between its output. The operation of the circuit is illustrated in Figure 1. Note that \( V_{\text{OUT}} = V_{\text{IN}}(+) \), and \( V_{\text{REF}} = 0 \). Substituting in the first equation, you obtain \( V_{\text{OUT}} = V_{\text{IN}}(+) - V_{\text{OUT}} \), or \( V_{\text{OUT}} = V_{\text{IN}}(+) \). Therefore, you have a divide-by-2 circuit. One of the interesting features of this approach is that the input and the output offsets of the instrumentation amplifier are divided by 2 as well.

You can implement the circuit on the bench using the LT1167 or the LTC2053 instrumentation amplifiers (Figure 2). Although benchtests are unnecessary, you can introduce an RC network into the feedback path for noise shaping and to guarantee dominant-pole behavior. To test for LT1167 offset, set \( V_{\text{IN}}(+) \) to 0V and alternate \( V_{\text{IN}}(-) \) between 0V and \( V_{\text{OUT}} \). This test confirms that the feedback halves the total offset voltage. Dividing 10V to 5V, the LT1167 shows an error of 100 μV. With the more precise LTC2053, the output error in dividing 2.5V to 1.25V is an almost-immeasurable 2.5 μV. Using cold spray and a heat gun, you can degrade this error to 15 μV. However, perhaps equally important are the calculated worst-case results.

Worst-case calculations for the LT1167 show a maximum 1.12-mV error over 0 to 70°C with 10V input and 5V output. This figure constitutes a total error of 224 ppm over temperature. Resistors that guarantee this accuracy would need a maximum tolerance of 112 ppm each over temperature. The error budget of a resistor-divider solution would require an initial ratio match of approximately 50 ppm with a temperature-coefficient match better than 1 ppm/°C. Worst-case calculations for the LTC2053 with 2.5V input and 1.25V output show a maximum 80-μV error over 0 to 70°C. This figure constitutes a total error of 64 ppm over temperature. Resistors that guarantee this accuracy would need a maximum tolerance of 32 ppm each over temperature. The error budget of a resistor-divider solution would require an initial ratio match of approximately 15 ppm (0.0015%) with a temperature-coefficient match better than 0.25 ppm/°C. In either case, resistors of this caliber would be extraordinarily expensive if available at all. Also, the amplifiers provide the additional benefits of high input impedance and output buffering. Moreover, the error calculations include the effects of input offset voltage, bias current, gain error, and common-mode rejection ratio, which a resistor op amp would still have to add.