RECEIVER EQUALIZATION USES A TAILORED AMPLIFIER-TRANSFER FUNCTION TO COMPENSATE FOR TRANSMISSION-MEDIA LOSS AND PHASE SHIFT AT HIGH FREQUENCIES. YOU CAN CHARACTERIZE THE EQUALIZER’S PERFORMANCE WITH THE TRANSMISSION MEDIA USING EXTERNAL PHASE MODULATION OF INPUT DATA AT FREQUENCIES HIGHER THAN THE DESERIALIZER’S CLOCK-RECOVERY-LOOP BANDWIDTH.

Receiver equalization increases link distance without adding EMI

Receiver equalization and transmitter pre-emphasis in a SERDES (serializer/deserializer) can increase link distances in backplane and line-card applications. Receiver equalization has many advantages, such as lower EMI and easier adaptive implementation, over transmitter pre-emphasis. However, the use of receiver-equalization technology is less common than the use of pre-emphasis techniques. Most users are comfortable implementing transmitter pre-emphasis because they can directly observe the improvement on signal integrity after the link medium, or far end. Many system designers do not implement receiver equalization because it does not produce directly observable eye-pattern results, and designers cannot directly observe the improvement and margin in their systems. A bit of theory and an application example of a frequency-domain receiver equalizer show why receiver equalization can improve signal integrity, demonstrate how to characterize it, and give you a feel for how much eye distortion this technique can tolerate from measured real-life data.

A SERDES is a common transceiver for point-to-point high-speed connections. A serializer converts a low-speed parallel data bus into a high-speed serial data stream for transmission from point A to point B through the medium (Figure 1). A deserializer with a built-in CDR (clock-and-data-recovery) unit then converts the high-speed serial data stream back to its original parallel format. Figure 1 shows a simplex configuration because each node uses only half of a SERDES. Most applications require duplex configuration, for which each node uses a full SERDES and performs both serialization (transmission) and deserialization (reception). The SERDES reduces the number of wires required to transfer data between two nodes, resulting in a simpler system implementation and longer driving distance.

**Figure 1**

A serializer converts a low-speed parallel data bus into a high-speed serial data stream for transmission from point A to point B through the medium.
SERDES/transceiver combinations are common in backplane and line-card applications. The transmission media are usually cables of different configurations or microstrip traces on a pc board. The transmission medium has a finite bandwidth, which defines the maximum distance between transmitter A and receiver B at a given data rate.

For most applications, media-transmission characteristics are functions of frequency, and you can model them as follows:

\[ T(f) = \exp(-k_I (1 + j)\sqrt{f} - k_d f) \]  

where \( l \) is media length, \( f \) is frequency, and \( k_I \) and \( k_d \) are constants representing conductor and dielectric losses, respectively (Reference 1): At data rates lower than 3 Gbps, conductor loss dominates, so you can simplify Equation 1 to

\[ T(f) = \exp(-k_I (1 + j)\sqrt{f}) \]  

Equation 2 has both real and imaginary terms, indicating that the high-frequency component of the signal has not only higher attenuation, but also higher phase shift than its low-frequency counterpart. Both attenuation and phase shift are proportional to distance, \( l \), and \( \sqrt{f} \). Attenuation reduces the vertical eye opening at the receiving end. Phase shift at higher frequencies results in ISI (intersymbol interference), which introduces excessive timing jitter and ultimately limits the maximum transmission distance. For example, the eye opening of ideal 500-mV, single-ended peak-peak PRBS-7 pattern at 3.125 Gbps is completely closed after transmission through a 20m Belden 8262 coaxial cable.

In the s-domain, Equation 2 is

\[ T(s) = \exp(-k_I (1 + \sqrt{s} f)) \]  

An amplifier with a transfer function that’s the reciprocal of Equation 3 can correct the media-frequency dependency. Ideally, this amplifier has the following transfer function, \( H(s) \):

\[ H(s) = \frac{1}{T(s)} = 1 + \alpha \sqrt{s} \]  

You can implement this transfer function in a feed-forward system with a variable-gain, 10-dB/decade amplifier (Reference 2, Figure 3). With proper adjustment of the boost factor of the amplifier, the transmission system comprising the media and the amplifier can be frequency-independent. If you place this amplifier at the transmission point A of the link, the result is called pre-emphasis; if you place it at the receiving end, you call it receiver equalization. For example, the BBT3400 quad 3.125-Gbps/channel transceiver (www.bitblitz.com) has receiver equalization with 16 programmable boost factors, followed by CDR (Figure 4).

**RECEIVER EQUALIZATION HAS ADVANTAGES**

Receiver equalization has certain advantages over pre-emphasis. For example, at high boost levels, electromagnetic interference is less significant than in pre-emphasis because the system doesn’t boost a high-frequency signal at transmission. An adaptive system is easier to implement because you set the boost factor at the receiving end. However, although pre-emphasis produces a clear eye opening at receiving, the output of the...
equalizer is usually an internal node, and a special laboratory setup is necessary to characterize equalization performance. For example, you can use the BBT3400-based design of Figure 4 with the equalization set to high boost to recover a data eye with less than $10^{-12}$ bit-error rate, but the received data eye provides no information about input-jitter-tolerance margin. Knowledge and the guarantee of enough input-jitter-tolerance margin are important for designing a robust system. You can measure the input-jitter-tolerance margin by phase-modulating the input data until the bit-error rate reaches $10^{-12}$ (Figure 5). Figure 5’s scheme loops back the BBT3400 serializer to its deserializer through a parallel interface. The bit-error-rate tester, generates data patterns that travel through the transmission media, the BBT3400, and its error detector for bit-error rate measurement. A phase modulator modulates the bit-error-rate clock source with a sinusoidal wave. If the modulation frequency is higher than the deserializer CDR unit’s loop bandwidth, the maximum phase modulation is the input-jitter-tolerance margin. In the case of the BBT3400 receiving a 3.125Gbps PRBS-7 pattern through 20m Belden cables, as much as a 0.5-unit-interval high-frequency modulation is possible with a bit-error rate of less than $10^{-12}$. One unit interval equals 320 psec for 3.125-Gbps NRZ data. The input data eye is more than completely closed (Figure 6). The phase-modulation measurement concludes that, with the help of receiver equalization, the BBT3400 can tolerate approximately one unit interval of input ISI jitter with a 0.5-unit-interval margin at $10^{-12}$ bit-error rate. In other words, the BBT3400 has a greater-than-0.5-unit-interval margin in recovering data from Figure 4.

**References**


**Author’s Biography**

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