The flat-panel-display industry is changing, as several industry groups and vendors propose varying digital standards for connecting the PC's graphics adapter to the display. A problem remains, however: These standards are incompatible with the several hundred millions of analog graphics cards in the PC world. Thus, flat-panel-display vendors must face the challenge of designing complex interface requirements for analog compatibility. Thus, several interface schemes work, but each offers different technical and marketing advantages. And, so far, none of the approaches has gathered enough momentum to become a dominant standard.

Digital transmission provides the highest possible image quality, and you can easily upgrade it to handle future requirements. However, digital standards are emerging only now, and two factors are threatening to slow their adoption: First, the industry is still undecided on which digital format to use. The transition-minimized differential-signaling

SEVERAL TECHNICAL APPROACHES ARE VYING TO BECOME THE STANDARD INTERFACE BETWEEN COMPUTERS AND FLAT-PANEL DISPLAYS. WHILE THE INDUSTRY SEARCHES FOR HARMONY, THE APPROACHES ARE HIGHLIGHTING THE CHALLENGES OF MAKING FLAT-PANEL DISPLAYS PLUG-COMPATIBLE WITH CRTS.

COMPEING STANDARDS seek common ground for flat-panel displays

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(TMDS) protocol from Silicon Image has now emerged as the leading protocol for the digital interface in desktop PCs (Figure 1), whereas National Semiconductor’s low-voltage differential-signaling (LVDS) protocol-based FPD-Link is ubiquitous in the notebook-PC industry. Second, flat-panel-display vendors hesitate to deploy digital monitors until widespread adoption of the digital connector on PCs emerges. Also, except for Compaq (www.compaq.com), which implemented the digital-flat-panel (DFP) standard in its Presario series, PC makers have been slow in adopting the digital standards.

Two recently proposed standards in the United States, the Open LVDS Display Interface (OpenLDI) and the Digital Video Interactive (DVI), and one in Japan, the Gigabit Video Interface (GVIF), have provided a momentum for faster adoption of flat-panel displays. National Semiconductor recently proposed the OpenLDI standard, which relies on an LVDS interface, in which a transmitter serializes the parallel pixel data and sends it from the PC to the flat-panel display. There, a receiver returns the pixels to their parallel format. Unlike both TMDS and OpenLDI protocols, which use several pairs of differential signals for data transmission, the GVIF protocol uses a single pair of differential signals to transmit data.

The Digital Display Working Group, an open industry group comprising Compaq, Fujitsu (www.fujitsu.com), Hewlett-Packard (www.hp.com), IBM (www.ibm.com), Intel (www.intel.com), NEC (www.nec.com), and Silicon Image proposed the TMDS-based DVI specification. The TMDS link sends graphics data to the monitor. An advanced encoding algorithm minimizes signal transition by converting 8 bits of data into a 10-bit transition-minimized, dc-balanced character.

DVI uses the Video Electronics Standards Association (VESA, www.vesa.org) extended-display-identification-data structure for identifying the flat-panel display’s type and capabilities. It allows for the BIOS power-on self-test and allows the OS to query the monitor using the display-data channel protocol to determine what pixel formats and interface the display supports. DVI provides single- or dual-link implementations. The single link can support greater than high-definition-TV (HDTV) formats of 1920×1080 pixels at reduced blanking intervals. The dual-link configuration supports higher bandwidth demands of displays that do not support reduced blanking. The dual-link configuration also supports large-pixel-format digital CRTs, which are similar to classic CRTs except the graphics controller receives digital graphical data and the final D/A conversion occurs in the monitor.

Both VESA plug and display (P&D) and Compaq’s digital-flat-panel standards employ the TMDS protocol and can interoperate with DVI via a connector adapter. DVI uses a connector shell that provides either DVI-V digital-only implementation for use with legacy VGA or DVI-I integrated implementation, which includes analog RGB for workstations. The 30-pin connector provides 29 connections, comprising 18 TMDS wires and shields, five plug-and-play connections, and six RGB-and-return and horizontal/vertical signals.

Silicon Image offers the DVI-compliant SiL160 transmitting and SiL161 receiving chip set that uses PanelLink Digital technology to interface displays ranging from 640×480-pixel VGA to 1600×1200-pixel UXGA resolutions at 25 to 162 MHz. The chip set supports true-color panels as large as 24 bits/pixel, 16.7 million colors, one- and two-pixel/clock modes, and an interpair skew tolerance as great as one full input-clock cycle of 15 nsec at 65 MHz. Both chips comply with VESA P&D, VESA flat-pan-

**Figure 1**

A TMDS transmitter encodes and serially transmits an input data stream over a TMDS link—comprising three encoders, each driving one serial TMDS data channel—to a TMDS receiver. Depending on the state of the data-enable (DE) signal, the encoder produces 10-bit TMDS characters from either the two control signals or the 8 bits of pixel data.
Flat-panel-display interfacing

The OpenLDI LVDS signal lines support a minimal 1-nsec bit time. This time corresponds to a 142.8-MHz pixel-clock rate. You can apply pre-emphasis to the LVDS signal lines to achieve reliable communication when using longer cables.

THE GVIF STANDARD

Sony last year proposed the GVIF protocol, a 1-bit serial data system based on a 1.56-Gbps, PLL-based, serializer/deserializer technique. The GVIF integrates a simple encoder-decoder and a self-control system on a single-chip transmitter and a single-chip receiver. In contrast, high-speed serializer/deserializer systems, such as 1.06-Gbps Fibre Channel, 1.25-Gbps Ethernet, and 1.48-Gbps Serial Data Interface, require external encoders/decoders, controllers, reference clocks, or cable equalizers for transmission. In addition, the GVIF-receiver chip also integrates a cable-equalizer circuit, which allows the chip to transmit XGA-resolution video via one 5-mm-diameter, more-than-20m-long differential cable without optical fibers or special cables. At higher resolutions, such as SXGA and UXGA, GVIF uses two pairs of differential signals through the cable.

GVIF-CODING TECHNIQUE

Sony based the GVIF’s encoder/decoder scheme on 3B4B (four signal transitions for each of 3 data bits) encoding, in which the encoder translates 18-bit RGB data and 6-bit synchronization/control signals into a 24-bit word for serial NRZ data transmission. Using a self-control-circuit scheme, GVIF achieves hot-pluggability functions: The self-control circuit helps the cable driver to lock into serial data without off-chip controllers or reference clocks. GVIF uses a common-mode voltage of the differential cable to acknowledge cable-driver status, and the transmitter temporarily sends reference signals to help the receiver to lock in.

I-O Data Device Inc. has developed the

The D590C387 OpenLDI transmitter at the host graphics controller serializes 24 or 48 bits of pixel data and transmits over five LVDS pairs for single-pixel formats or 10 LVDS pairs for dual-pixel formats. At the flat-panel-display end, the DS90CF388 OpenLDI receiver converts these LVDS signals into parallel form and outputs them to the flat-panel display.
Flat-panel-display interfacing

$100 GA-TR02G4/PCI GVIF-development board. The highly integrated digital graphics boards for LCD monitors provides GVIF-compatible output on a 14-pin MDR (mini-delta-ribbon) connector and analog RGB on a 15-pin D-sub connector. The board supports resolution as high as SXGA.

**CROSS-POLLINATION AMONG STANDARDS**

The DVI standard employs several components from other interface standards. For example, DVI endorses a connector that is similar to VESA's plug-and-play standard. DVI also borrows the double-width-channel idea from National and TI's LDI standard. Likewise, National has incorporated the dc-balancing scheme from TMDS for a robust transmission of digital data in a flat-panel-display interface.

As for connectors, DVI goes further by reducing the number of signals in the protocol by eliminating Universal Serial Bus, IEEE-1394, and audio signals. Also, DVI's dual-input, analog-and-digital-option transitional strategy could promote the standard's adoption in both the LCD-monitor and the CRT markets.

**SPECIALIZED ASICs**

A huge design opportunity exists for specialized ASICs that eliminate trade-offs between analog VGA and emerging digital standards by accommodating both analog- and digital-video connections between the PC. Specialized ASICs can include spatial processing (image scaling and resolution conversion), temporal processing (timing conversion to synchronize with the optimal range of the flat-panel display), color-depth processing (transforming colors to those the display supports), and automatic mode detection and switching.

For example, the Arithmos ADE2000 series display engines simplify the flat-panel-display interface. The ADE2000 series integrates automatic synchronization-detection circuitry, a triple-high-speed video ADC (on the model 2100 only), frame conversion, an on-screen-display generator, a proprietary IQ-scaling engine, and the company's PerfectColor processor. The ADE2100/ADE2200 support dual analog and digital inputs with autosensing and switching. The IQ-synchronization feature uses adaptive detection of the video data to exactly reproduce the digital source and avoid artifacts, such as loss of sharpness and misalignment. IQ synchronization can identify known modes and set up the monitor parameters. Also, for unknown modes, the IQsync processor can still identify the timing parameters and calculate the appropriate settings on the fly.

The ADE2100 with input rates as high as 95 MHz supports XGA-resolution LCD panels, and the ADE2200 with input rates as high as 135 MHz supports SXGA-resolution LCD panels. The devices cost $44 (5000) and $59 (5000), respectively, and costs $45 for the 135-MHz version. Sage's SureSync and SmartSet proprietary technologies characterize an input signal and extract its resolution information, refresh rate, image position, and phase. Using this information, the device synchronizes the signal, using either on-chip or external ADCs. If your design needs frame-rate conversion, you can use external synchronous DRAMs as frame buffers. Cheetah3 is available in a 240-pin PQFP and costs $35 (1000) for the 95-MHz version and $45 for the 135-MHz version. Cheetah3's scaling algorithms use a hard-wired DSP based on an interpolation-algorithm technique, according to Tammy Michel, marketing manager for IC products at Sage. The Cheetah3's autoset/autoadjustment feature enables automatic adjustment of horizontal/vertical position and clock phase.

The Bridge 120 chip from Paradise Electronics lets you unplug CRTs and plug in flat-panel displays without modifying the PC. The Bridge 120 integrates three ADCs, a PLL, a scaling engine, and panel-interface logic. The 160-pin PQFP device supports 1280×1024-pixel SXGA resolution and requires no external frame-buffer memory. The Bridge 120 costs $35 (1000).

Similarly, the 160-pin, PQFP-housed SD1000B from SmartASIC Inc, an analog-interface, XGA, TFT LCD controller automatically detects input mode and automatically calibrates the phase without external CPU assistance. Six channels of 8-bit ADCs first sample the analog-input RGB signals and feed the RGB data into the SD1000B. The SD1000B then automatically scales the input image to fit the full screen of the LCD monitor. Implementing timing parameters in external EEPROM eases interfacing with various manufacturers' TFT LCD panels.

No matter which standard wins, vendors agree that it will take a long time before a common standard exists. Sage's Michel sees a lot of momentum behind the DVI standard. In the short term, she says, her company's products will accept digital TTL input and leave it to the customers to implement the LVDS or DVI.

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**Figure 3**

Unlike the TMDS and OpenLDI protocols, which use several pairs of differential signals for data transmission, the GVIF protocol uses a single pair of differential signals to transmit data. The GVIF coding encodes 24-bit RGB data plus a 6-bit header into a 30-bit code for data transmission.
interface. Arithmos’ Soderberry agrees. “DVI is not yet finalized, and the connectors will not be available for some time,” he says. “Most vendors are doing P&D, DFP, and alternative solutions, and we see a period of proprietary techniques with the focus on DVI.” However, Soderberry says that the various standards adequately serve the market’s needs when delivering digital bits from the PC to the monitor.

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