Today’s most advanced low-voltage microprocessors, DSPs, and PLDs use two power supplies of different voltages to significantly reduce power requirements. Proper sequencing can mean the difference between dual supplies and dueling supplies, with system reliability hanging in the balance.

Power-supply sequencing for low-voltage processors

The use of a dual-voltage architecture often requires coordinated management of both supplies to avoid potential problems with device and system reliability. Designers must consider the relative voltage and timing of core- and I/O-voltage supplies during power-up and -down operations to comply with manufacturers’ requirements. Intelligent, dual-output-supply control ICs are useful for sequencing power supply rails in low-voltage systems.

Why Sequencing Matters

Sequencing refers not only to the order in which voltage rails power-up and -down but also to their timing and voltage-differential relationships. Designing a system without proper sequencing risks two kinds of potential danger. The first type represents a threat to the long-term reliability of the dual-voltage device. The second can cause either immediate or latent faults and possibly damage I/O ports in the processor or supporting system devices, such as memory, logic, or data-converter ICs.

The threat to long-term reliability of the dual-voltage device comes from the possibility of breakdown in the ESD protection and well-isolation structures that internally separate the two power-supply rails. If one rail is active while the other is inactive, damage may occur if the condition persists for extended periods. It is important to realize “extended periods” mean months for most devices, a time scale that does not apply to ordinary design considerations for these systems. However, device manufacturers count the cumulative lifetime exposure to conditions under which a processor operates with a single powered rail. It is unlikely for a single or even several poorly controlled power-up and -down cycles to harm the processor. But in a system that is power-cycled many times a day, day after day, the dual-voltage device’s operation may ultimately suffer from a compromised long-term reliability.

By contrast, improper supply sequencing can cause immediate and catastrophic damage to the bi-directional I/O ports. With most ICs fabricated in CMOS technology, the potential for latch-up exists when a processor’s I/O port and the I/O port of a supporting peripheral, such as memory, an FPGA, or a data converter, do not share the same supply.

Latch-up occurs when current forced through the substrate of a CMOS device triggers a self-sustained conduction path in back-to-back parasitic bipolar

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**Power-supply sequencing**

**VOLTAGE (V)**

**TIME (mSEC)**

Sequential power-up imposes a fixed delay between supply ramps or ramps the second supply after the first reaches regulation.
transistors (as in an SCR). Current continues to flow until the device fails or until the supply powers down. The trigger current may occur if a supply powers one device, enabling it to source or sink current into or out of the second device before the second device fully powers up. A latch-up condition may cause damage that is immediately noticeable, or it may affect reliability over a long period of time. To handle latch-up problems, you must power any logic peripheral connected to the processor I/O bus from the same supply rail that powers the processor’s I/O section.

Bus contention occurs when the processor and another device simultaneously attempt to control a bidirectional bus during power-up, which can affect I/O reliability. Designers should check the specifics for bus contention for individual devices. To eliminate the risk of these dangers to the processor and system ICs, good design practice provides careful power-up and power-down sequencing.

**APPROACHES TO POWER-UP SEQUENCING**

To avoid potential threats to the processor and system ICs, designers follow three general methods for power-up sequencing. Taken together, these design approaches are referred to as power-up sequencing methods, a term that should not be confused with sequential power-up.

Sequential power-up, as its name implies, energizes the two rails one after the other (Figure 1). Typically, the second rail begins to ramp up once the first rail reaches regulation. Alternatively, the second rail may begin its ramp after a set delay from the start of the first rail. Both methods must comply with manufacturers’ restrictions on the minimum or the maximum lag time or with the duration and amount that one supply exceeds the other. With the second method, the ratiometric method, the two rails begin to power up and reach regulation at the same time (Figure 2). This method requires a higher slew rate for the rail with the higher final voltage and results in the maximum voltage differential when the supplies reach regulation. However, some processors may not tolerate the instantaneous voltage differences that occur while the supplies are slewing. The third approach eliminates instantaneous voltage differences. A common way of implementing the third method is simultaneous power-up, in which the voltage rails rise together and at the same rate, with the higher or I/O voltage rail continuing after the lower or core voltage rail has reached its final value (Figure 3).

In general, microprocessor manufacturers do not specify which sequencing method the power-subsystem designer should use; they simply specify restrictions on time or voltage differences during power-up. Some processors allow out-of-tolerance voltage conditions to persist for just 50 µsec, and their data sheets recommend diodes between the core and the I/O rails to prevent the out-of-tolerance conditions in the absence of coordinated power-up of the core and I/O rails. Data sheets for other processors do not define the restrictions as well. Although they may not specify a specific order for powering the voltage rails, system designers should consider bus-contention issues. Good design practice may call for powering up both rails at the same time or powering up one rail before the other to prevent unknown output states on the I/O bus. At least two device manufacturers, Intel and TI, caution against leaving only one supply powered for long periods. Although vendors do not often specify a maximum period, a useful rule of thumb is to complete powering up or down both rails within 1 sec. This time period is chosen for convenience; it is significantly longer than the time needed to accomplish the task but much shorter than the time that would damage the device from having only one rail active, even if the damage is cumulative.

**PRACTICAL SEQUENCING**

Although the restrictions on simultaneous power-up are greater than on other power-up methods, all of the methods require coordinated control of the two power supplies. Until recently, designers have accomplished this coordination through the use of diodes connecting the two power-supply outputs. With this technique, if one rail rises ahead of the other, it pulls the second rail along with it.

As long as the voltage rails are close together (for example, 3.3 and 2.5V), diodes can control the separate voltage ramps. However, core voltages of 1.8 and 1.5V are frequently used today, with
even lower voltages coming soon, whereas the I/O voltage is likely to stay at 3.3V for some time. With large voltage differentials between core and I/O, the diode technique is less effective because diode ratings are too inaccurate to produce a predictable voltage drop from one rail to another. Thus, it becomes necessary to use a different technique for power-up sequencing.

A straightforward design for sequential power-up would use a comparator, voltage detector, or SVS (supply-voltage supervisor) to monitor the first supply in the sequence and delay the power-up of the second. If the supply input equals the I/O supply, the voltage-monitor circuit could control a MOSFET switch or a low-dropout regulator operating in dropout mode. If the input supply is greater than the I/O supply, a regulator is required. Dual low-dropout regulators with built-in monitoring circuitry can supply both the I/O and the core (Figure 4). The SEQ pin selects the order of the output power-up. When both outputs reach regulation, the RESET function delays processor execution for 120 msec. The TPS701xx, TPS703xx, and TPS707xx low-dropout regulator families, which can supply 150 mA to 2A to the core or I/O rails, integrate these functions.

A simple implementation of ratiometric power-up sequencing consists of connecting the soft-start inputs of two switching-controller circuits to the same-sized capacitor. To make the rise times nearly identical, you may be able to connect both soft-start inputs to one capacitor. This situation is especially true if a single chip integrates both controller circuits. In this case, the characteristics of the soft-start inputs closely match, making it more likely that the outputs ramp up within a tight timing window. A dual-output switching controller, such as the TPS5102, with its PWM outputs, allows the use of a single external capacitor for ratiometric power-up. A dual-controller IC also allows the circuit designer to use capacitors of different sizes to predictably retard one of the output ramps.

Although you can use most power supplies with soft-start inputs for ratiometric power-up, simultaneous power-up requires a device with dual-level outputs that track to keep the timing matched within user-selected limits. As an example, the TPS56300, with a low-dropout regulator for I/O and a switching regulator for the core, integrates a single capacitor for both outputs and regulates them using the same reference voltage to provide tight matching (Figure 5).

The system designer should also account for power-down sequencing. The node capacitance and resistive load determine the voltage profile of each rail during power-down. But in typical digital systems, power-down can occur as a result of several scenarios, including situations in which the loading on either rail changes during power-down and is different from one power-down event to another. A technique for making the power-down rates occur more reliably involves discharging the power-supply outputs with a known load each time. The TPS563xx, TPS701xx, TPS703xx, and TPS707xx low-dropout regulator families integrate circuitry that provides an internal discharge path on each output. The circuitry activates automatically when the input supply falls below an undervoltage-lockout threshold or upon the receipt of a logic-shutdown signal.

GOOD POWER-SUPPLY DESIGN

As the use of dual-voltage microprocessors, DSPs, and PLDs increases, the gap between core- and I/O-voltage levels is widening. Soon, cores will be running at 1V or less, whereas I/O voltages are likely to remain at 3.3V for some time. In this dual-voltage environment, good power-supply-design techniques, such as proper sequencing, will be more important than ever. Sequencing helps ensure the long-term reliability of the processor and at the same time helps protect system-I/O cells. The processor in question may require strict timing and voltage differentials; nevertheless, it is desirable to design the power-supply rails to rise and fall predictably. Today’s intelligent, dual-output supplies help simplify designing power for the low-voltage processors that are fundamental to many types of systems.

Author’s biography

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