BY TAKING A DIFFERENT APPROACH TO SWITCHING-SUPPLY DESIGN, YOU CAN DEVELOP AN ARCHITECTURE THAT IMPROVES OVERALL SUPPLY PERFORMANCE IN CRITICAL TRANSIENT SPECIFICATIONS.

Modify your switching-supply architecture for improved transient response

Switching power supplies typically have tight static-regulation specifications. Using widely available precision references, you can easily achieve ±1% accuracy over the operating-temperature range without any initial adjustment. You also have to deal with the supplies' dynamic-regulation specification, which manufacturers typically specify as a maximum allowed deviation with a transient load that has a stated current step and a stated maximum allowed slew rate. These specifications, along with recovery time, define how long after the transient it takes the output voltage to recover to within the static limits.

Specifying a power supply to the best of its static-regulation capabilities works fine for general-purpose power supplies and applications. A string of two or three zeros trailing behind a 3V output measurement looks aesthetically pleasing, even if the load requires no such accuracy. It also is natural for you to assume that you can minimize the total dynamic peak-to-peak deviation by having those deviations originate from the most restricted static-regulation point. As a result, the specification and design effort for a switching power supply have evolved to maintain tight static-voltage specifications and require a recovery from load transients at the fastest reasonable rate. The implication is that the power supply has a high loop gain, and it therefore presents a challenge to the supply to provide quick transient recovery while maintaining adequate phase margin.

For voltage-mode-controlled power supplies, the double pole of the LC filter and the zero of the output capacitor with its associated equivalent series resistance (ESR) provide a challenge when you try to optimize the compensation. The variability of the filter parameters, especially the ESR, can play a big role in limiting how well you can optimize the loop. Current-mode control addresses the stability issue by controlling the current into the output filter rather than the average voltage into it. This approach eliminates the inductor from the loop but introduces the expense of a current sensor, which is typically a resistor. In cost-sensitive applications in which every penny counts, this resistor seems like an unnecessary expense that you could eliminate with a better loop design. This goal has led engineers...
to develop numerous nonlinear, voltage-mode-derived control techniques holding the promise of an ever-quickening high-gain response capability, which can correct a detected transient and return the supply to a tightly regulated static condition with a stable operating loop.

Consider a representative power requirement on a supply for a typical load: that its supply voltage be within a certain range, such as ±5% of a nominal value. The specification seldom has allowed additional deviation for transients, but the specs allow that static deviation is more than what the power supply is typically designed to achieve. For dynamic loads, such as a microprocessor, the load typically runs three orders of magnitude faster than the power supply switches, and its current-demand slew rate is correspondingly many times faster than what a switching power supply can achieve. Further, with the dynamic-power-management techniques that processors increasingly require, the microprocessor slews regularly between its maximum demand and nearly zero current demand with a high slew rate.

Because the power supply inherently cannot respond substantively with a change of current through the output filter, the full transient current magnitude, ΔI_{O}, appears suddenly in the output capacitors. Following this transient, the supply generates a relatively gentle recovery in a valiant attempt to quickly slew the current to meet the new demand of the load. Because an output capacitor’s impedance typical dominates the ESR, the transient-response voltage characteristic usually looks just like the current transient. In response to a full-load transient, you get a sudden jump or dip in the output voltage; a more or less linear recovery ramp follows this jump or dip. The magnitude of each deviation is ΔV_{O} = ΔI_{O} \times ESR, and, when you consider the ripple voltage due to inductor ripple current, ΔI_{L}, and power-supply tolerance errors, V_{ERR}, the peak-to-peak output-voltage containment that the power supply can achieve for this load (Figure 1) is:

\[ V_{PF} = V_{ERR} + (ΔI_{O} \times ESR) + \left( \frac{2 \times ΔI_{L} \times ESR}{(2 \times ΔI_{L} + ΔI_{O}) \times ESR} \right) V_{ERR} \]

(1)

This equation does not account for a possible nonlinear response of the supply to more quickly bring the voltage back to the static condition, but that situation is irrelevant because the damage to containing peak-to-peak output voltage has already occurred. The main goal of an optimal power-supply design for an application load is to contain this output voltage within the specifications that the load requires and at a minimum cost. Yet, power-supply control-device vendors emphasize higher switching frequencies and faster loops during transients, neither of which practically address this fundamental problem.

You can gain an intuitive understanding of the power supply’s load-transient performance by studying the simple equivalent circuit model (Figure 2). The main voltage source, V_{CC}, delivers the nominal voltage. Another series source represents errors in the power supply’s accuracy, and, because the error is bide-rectional, the polarity of this source is unknown, and you must accommodate it. You should also include the ripple-voltage error in this source. The resistor value is the ESR. Finally, there is an equivalent output inductance that limits the slew rate of the power supply. For a buck converter, that equivalent inductor is: I_{EQ} = I_{O} (ΔI_{MAX, ESR}/V_{LMIN}), where V_{LMIN} is the lower of V_{O} and V_{IN} - V_{O}.

It’s reasonably straightforward to derive the preceding formula by inspecting this model. Note that this approach attempts to solve the problem by, in effect, lowering the equivalent-inductance value. If you could make this equivalent inductance low enough to give the power supply a slew-rate capability close to that of the load, this approach would be valid for containing voltage transients. But, because that case does not apply to this example, reducing the equivalent inductance in the model hardly affects transient containment.

You can gain several benefits by addressing the 2× factor in Equation 1 when designing the power supply rather than designing it to just maintain the tightest fixed voltage that you can achieve under static conditions. What would happen if the low-to-high and high-to-low transients did not originate from the same static-regulation voltage, and how can you optimally implement such a regulation system?

By examining various power-supply topologies and control techniques, you conclude that the ESR is inevitable, and you cannot substantially lower it without the expense of additional bulk-output capacitors. Furthermore, studying the output filter in these applications typically shows that you require an abundance of capacitors simply to obtain a sufficiently low ESR to constrain the severe transients. Once you accept the ESR as an impedance that inherently causes a minimum deviation of ΔV_{O} whenever a load transient occurs, you see that the inductance brings the voltage back to the starting point, which is why the equation requires a factor of 2. This feature is the one that power-controller providers have been addressing incorrectly. If you cannot reduce the equivalent inductance to provide substantial slew rate from the power supply during a load transient, then arbitrarily lowering the inductance...
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Figure 4

The load-transient response of the ideally voltage-positioned supply shows that the voltage dips after a load increase and quickly jumps back after the load decreases.

Figure 3

Another undesirable feature of this implementation is that the supply passively accomplishes the voltage positioning by pc-board-trace resistance or by the use of a discrete resistor. This resistance must produce the entire voltage drop. The power dissipation of this resistor may become a problem when the desired resistance is large. The term “passive-voltage positioning” distinguishes between this technique and the hybrid technique, which is disappointing to the scientific mind. Further, the application literature usually recommends an ambiguous droop-resistance value that is substantially less than what it ought to be, which is also disappointing to the scientific mind. This ambiguity probably exists because no one has satisfactorily explained the resulting reduced load-regulation characteristic, and, thus, the droop resistance still carries a mark of poor performance. An arbitrary and poorly controlled compromise usually exists between the correct voltage positioning and designers’ habitual desire to tighten the load regulation.

Another fundamental but problematic characteristic of this technique departs from the ideal model. Consider a no- to full-load transient, beginning from a static condition. The initial transient current first flows from the output capacitors, and the output voltage dips accordingly. At first, the power supply still does not substantially increase its current, so it sees no voltage drop across the droop resistance and thus responds to correct the output voltage back to the zero-load regulation level. This situation creates a linear ramp-up of current in the output filter. Because of the ESR of the impedance that exists on most converters’ aluminum-electrolytic capacitors, this ramp-up of current immediately creates a linear ramp-up of output voltage after

does not increase performance. You must instead look the other direction: making that equivalent inductance so infinitely large that the model eliminates it.

Consider the response of the power supply in the same application if you eliminate the equivalent inductance from the model. Because the output voltage does not decrease at higher loads when drawing current through the ESR, consider placing a small positive-offset voltage in series with the equivalent output-voltage source, $V_{CC}$, that causes the output voltage to start out above nominal. Then, as it loads up to maximum current, the output voltage decreases to a below nominal value. This characteristic is equivalent to a supply that has poor load regulation, which is objectionable if you follow the stereotypical ideal objective for the power supply, which assumes that you should sum all error sources.

This model now appears to be an ideal power supply, including errors and offset, with some resistance in the positive-connection cable (Figure 3). When you remove the inductance, the power supply now does not attempt a recovery after a load transient. Its voltage merely goes down after a load increase and increases after a load decrease (Figure 4). Perhaps surprisingly, the peak-to-peak transient containment now decreases to:

$$V_{pp} = dV_{ESR} + (dI_{ESR} \times ESR) + (\Delta I \times ESR)$$

$$= dV_{ESR} + [(\Delta I_{ESR} + \Delta I_{ESR}) \times ESR].$$

Despite the aesthetically displeasing output-voltage variation with load, the advantage of this model over that of the previous one is substantial. It contains the output voltage between the same limits with nearly twice as much ESR, and the error source and ripple voltage become small when you compare them with the allowed deviation, which is often the case. Nearly twice the ESR means nearly half as many output capacitors, substantially reducing cost and size. The remaining question is: How do you design a power supply to have this characteristic?

One approach is to loosen the load regulation to help contain load transients. However, this approach suffers from load-transient bandwidth limitation and inaccuracy. Therefore, to convey the potential benefits from what appears to be poor load regulation, you can use a voltage-positioning approach. Although using this approach is insufficient to achieve the performance of the optimal power-supply model, it can provide insight into how you must modify the power supply.

The most straightforward way to implement voltage positioning is simply to add some series resistance between the fixed-voltage-regulation point and the load. Adding resistance between the output capacitors and the load would defeat the purpose of reducing transient containment. You should instead add resistance between the inductor and the output capacitors. This approach then regulates the output voltage at the junction of the added resistor and the inductor and so decreases with increasing load. Only the output capacitors source the initial transient current and thus create a voltage drop proportional to the ESR, which is presumably no smaller than necessary. As a result, it is also desirable for the circuit to reduce its output voltage in the same proportion after the transient settles. This situation means that the added, or “droop,” resistance should equal the ESR, which you would expect after you examine the model.

This implementation yields disappointing results if you improperly choose or control the added droop resistance. This factor partially explains the unenthusiastic reception of the most common voltage-positioning technique: using trace resistance to create the voltage drop. Trace resistance typically has poor tolerance over pc-board manufacturing lots and temperature. It might also be difficult to produce sufficient resistance by pc-board layout if that resistance must be large.

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the load transient causes the dip. This situation does not continue indefini-
ately. The inductor current eventually builds to the point at which it is handling half of the load current, and the other half of the current still flows from the output capacitors. At that point, the output voltage regulates at the approximate midpoint between where the voltage started out and where it was after the initial dip. But the voltage cannot settle there, because the capacitor is still providing current. The voltage then settles back to the initial-dip level with an exponential decay and a time constant equal to the product of the capacitance of the output capacitor and the sum of the ESR and the droop resistance (Figure 5).

Thus far, you can easily contain the voltage within reduced limits similar to those of the ideal model, but the output impedance of the power supply is not resistive. The output voltage bounces before settling after a transient. The problem occurs when the load-transient repetition rate is such that a reversal of the initial transient occurs during the bounce-back response time of the power-supply voltage. For typical microprocessor power-supply design, this time is 10 to 20 µsec, which is well within the time that the microprocessor could reverse its current demand. If this scenario occurs, the output voltage incurs a transient of the same magnitude as when the power supply settles, and this transient sends the output voltage beyond the limits you want to impose. The effect is bidirectional, and the resulting peak-to-peak transient containment is close to that of a power supply with no voltage positioning (Figure 5). Thus, you lose the benefits of passive-voltage positioning for transient containment when the repetition times between load transients are in the same range as the power supply’s response time.

An important clue tells you what to do...
by considering the tendency of the power-supply output voltage to bounce. This bounce-back characteristic occurs when the power supply over-responds to a transient. You need to provide a well-controlled slow-down of this response to achieve the “instantly settled” characteristic that would result from having a purely resistive output impedance. Similarly, you need not design the switching frequency of the power supply to push the switches to the limits of switching loss that they can tolerate.

If you proceed down a scientific route, you would analyze the power supply to determine how to compensate it. You would find that, to create a power switch with the desired performance, you must have a current-sensing element that is accurate enough to position the voltage. You also need a control loop that has load-current information to command the ideal response. Finally, you need a standard peak-current-controlled technique with a simple single-pole compensation, which is equal to the zero of the output capacitance and its ESR, and a limited dc gain.

With current information in the loop, you can use active rather than passive voltage positioning, regulating the output voltage as a function of load-current information that the loop can amplify as
needed to create the desired voltage drop. Using an Analog Devices ADP3152 power-supply-control IC, you can test the results of this optimal-active-voltage-positioning (OAVP) technique. The results of this experiment confirm that the IC has achieved the ideal model characteristic (Figure 6). The variation of the inductance with the load, which is common with inexpensive powdered-iron toroidal cores and which changes the ripple voltage, does not degrade the optimum transient performance.

An unexpected additional benefit of voltage positioning is a lower maximum load dissipation. The power supply attains its minimum voltage rather than just being regulated at the nominal voltage at maximum load. In digital loads, such as microprocessors, the current reduces proportionally to its supply voltage. This action results in a reduction in load dissipation by the square of the voltage. For a load with a 5% or more allowed supply variation, this reduction can in turn appreciably reduce the dissipated heat. Alternatively, this approach lets you raise the performance of a thermally restricted load in fixed thermal designs. Even the additional power dissipation of the resistor makes for a smaller total dissipation than with a standard power-supply design.

Successful implementation of an OAVP power supply and reliable prediction of its performance require nothing extraordinary from the controller hardware but do require that you follow a unique design and analysis procedure. With all the glamour surrounding faster and more exotic power-supply-response control architectures, you might not expect that the fast-transient-containment performance leader is an unpretentious but not necessarily fast, easily compensated power supply that appears to suffer from poor load regulation. But you can get all these features and more, including lower maximum load dissipation, which leads to increased system reliability and is the key to better system performance in power-limited applications, such as microprocessors.

**TEN STEPS TO CONTROL CONFIGURATION**

Control-configuration and -component selection are unique to the power-supply controller’s configuration, but you can follow this general 10-step outline:

1. Determine the voltage-regulation specifications the load needs. This specification also defines a gross-voltage-regulation window.
2. Choose the switching frequency and the inductor to give an acceptable ripple current. You check the inductor value against the output capacitance to determine whether you need to reiterate the test.
3. Choose a current-sensor value. If the current sensor is a resistor, as is likely, choose a value that gives an acceptably large signal level and an acceptably limited maximum-power dissipation.
4. Determine the net regulation window by subtracting the error sources of the power supply from the gross-voltage-regulation window. The error sources are usually bidirectional, so you must subtract most errors from both the upper and the lower sides of the window. If the current sensor is a resistor, the regulation error that it produces is zero at no load (that is, on the upper side of the regulation window) but may reach maximum error at full load.
5. Determine the maximum acceptable ESR and maximum acceptable power-supply output resistance according to the formula $V_{\text{REG,NET}} = \frac{\Delta V_{\text{REG,NET}}}{(\Delta I_{\text{MAX}} + D)}$, where $\Delta V_{\text{REG,NET}}$ is the net regulation available for regulation, $\Delta I_{\text{MAX}}$ is the maximum output current, and $D$ is the ripple current. Note that only the ESR of the bulk output capacitors counts. You cannot consider the ESR as lower when you add lower-ESR ceramic capacitors in parallel, for example.
6. Select the output-capacitor type, preferably using the lowest voltage to allow the highest capacitance in a case size and determine how many units in parallel you need to meet the maximum ESR limit.
7. Determine the voltage level, $V_{\text{OUT}}$, at which the power supply must regulate at no load. This figure is the top of the net regulation window minus half the ripple current times ESR.
8. Determine whether sufficient capacitance is available, according to the formula $C_{\text{OUT,MIN}} = \frac{V_{\text{OUT}} \times \text{ESR}_{\text{MAX}}}{\Delta V_{\text{REG,MIN}}}$, where $L_{\text{MAX}}$ is the maximum inductor value and $V_{\text{OUT}}$ is the lower of the applied inductor voltages that limits the slew rate, that is, the lower of $V_{\text{IN,MIN}}$ and $V_{\text{IN,MAX}} - \Delta V_{\text{REG,MIN}}$, where $V_{\text{IN,MIN}}$ is the minimum input voltage. If the capacitance is insufficient, then you must use either a capacitor with a larger time constant or a lower inductor value and increase the frequency if necessary to avoid higher ripple values.
9. Use the inductor-current information with the needed loop-gain value to adjust the output voltage to start at $V_{\text{OUT}}$ and reduce by $\Delta V_{\text{REG,NET}}$ as the load increases to its maximum.
10. Filter the current control signal with a pole equal to the reciprocal of the time constant of the output capacitor. You can easily tune up the design’s performance. Tune the offset at no load and the voltage-positioning gain at full load. If the full-load output-voltage transient bounces back when the ESR is at its maximum value, then increase the compensation capacitance. If the output has additional overshoot after the initial transient, then you must decrease the compensation capacitance.

Reference


Authors’ biographies

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