Simple circuit prevents processor latch-up
Michal Kobylecki and Wojda Wlodzimierz, MK Design, Warsaw, Poland

The circuit in Figure 1 uses a Dallas Semiconductor DS1820 one-wire digital thermometer in a multipoint temperature-measurement system. The DS1820 sensor allows distributed temperature measurement and uses only one wire for both data communication and the power supply. You can easily connect the one-wire interface to a μC (in this example, a PIC16C63). The application accommodates as many as 16 DS1820 sensors in a 100m-long network, dubbed MicroLAN by Dallas. Unfortunately, with such long wires near high-current power cables, inductively coupled high-voltage peaks can cause μC latch-up, because the transient-voltage suppressor, D1, cannot limit the line voltage below 9.8V. The interface circuit in Figure 1 prevents such faults.

The sensor needs only one data line, but the interface circuit in Figure 1 needs two CPU-control signals. The first is the inverted-output data line, connected to transistor Q1 through resistor R3. If this line is at logic 1, the sensor’s data line connects to ground. Otherwise, resistor R4 pulls the sensor’s data line to 5V. If the sensor transmits data, the μC captures the data via R5. If an overvoltage peak occurs, R5 prevents μC latch-up by limiting the current to the μC pin. During the temperature conversion, the DS1820 needs an effective pullup circuit to provide an accurate conversion. Transistors Q3, Q4, and R provide an effective pullup function, which the μC activates by grounding the input signal to Q3.

The pullup function also improves the rising edge of the transmitted data. If the sensor connects to the μC through a long wire, the capacitance of the line degrades the rising edge of the data signals, because of the line-capacitance-R4 time constant. The short pulse from the pullup circuit improves the signal’s rising edge. It’s obvious that, when the pullup circuit turns on, Q3 must be off. However, the circuit protects itself against unintended signal corruption. If Q3 is open, the power voltage does not connect to the sensor’s data line. If you replace R4 with a 1-mA current source, you can obtain effective data transmission with lengths as great as 500m (empirically verified). (DI #2317).

A simple three-transistor circuit provide both latch-up protection and signal conditioning in this one-wire sensor/μC interface.
Dual one-shot makes rising- and falling-edge detector
Santo Camonita, Catania, Italy

The design in Figure 1 is an upgraded version of the circuit in a previous Design Idea (“Edge detector runs off single supply,” EDN, Dec 4, 1997, pg 140). It has fewer components, draws less current, and has higher input impedance. The circuit uses a 4098 dual monostable multivibrator with both sections connected. The circuit generates a pulse on both the rising and the falling edges of a signal. The duration of the output pulse is \( T = 0.5 R_2 C_2 \). \( R_1 \) and \( C_1 \) provide power-on reset. The circuit has another advantage: It provides two independent true outputs (Q1, Pin 6 and Q2, Pin 10) and two independent complementary outputs (\( Q_T \), Pin 7 and \( Q_T \), Pin 9). (DI #2316).

To Vote For This Design, Circle No. 396

Simple circuit measures diesel’s rotations per minute
David Magliocco, CDPI, Scientrier, France

You may find it useful to measure a diesel engine’s rotations per minute to accurately adjust the idling or to compare the motor’s speed under hot and cold conditions, for example. Not all cars or trucks come with a tachometer. The scheme in figures 1 and 2 allows you to measure rotations per minute with a DMM or an oscilloscope. In Figure 1, a piezoelectric sensor and an alligator clip, fastened directly to one of the four metal fuel pipes, detect the fuel-injection pulses. The piezo element generates a signal that connects to the signal-conditioning electronics in Figure 2 through a coaxial cable. The circuit uses a charge amplifier.

IC1, a versatile ICL7611 chosen for its high input impedance, low bias current,
and reasonable power consumption, acts as an inverting current-to-voltage converter. C₁ integrates the high-dV/dt sensor signal. R₁ ensures that the output of IC₁ is high in the absence of a signal. You must use high values for R₂, R₃, and R₄. The two diodes at the input protect the amplifier against overvoltage spikes. R₅ and R₆ create a virtual ground, so the circuit uses the full common-mode input range of IC₁. Figure 3 shows an oscilloscope trace of the amplifier’s output. The three small peaks between the main pulses are parasitic and come from the injection pulses of the other cylinders. You can fine-tune the shape of the signal with C₁. A value near 1 nF yields a smooth signal with low amplitude; a value lower than 100 pF gives a noisy signal with narrow pulses. The value for the trace in Figure 3 is 100 pF.

From one vehicle to another, the amplitude of the signal can vary over an approximately 2-to-1 ratio. You can’t use a fixed threshold to shape the signal; either the threshold is too low, and you shape the parasitic pulses, or it’s too high, and you obtain nothing. Thus, the signal-conditioning method compares the peak value to the average value: Only the main peaks are higher than the average value. C₂ and R₇ ignore the dc component of the charge amplifier’s output signal, and transistors Q₁ and Q₂ charge C₃ to the peak value of that signal. You adjust R₅ and R₆ for a 90% ratio, which gives IC₂, a low-power CMOS comparator, a large enough signal to shape. IC₂ delivers a log-like signal that you can measure with a DMM (using the frequency/period range, or the rotations-per-minute range on an automotive DMM), or with an oscilloscope. (DI #2318).

To Vote For This Design, Circle No. 397
Fast, compact routine interfaces EEPROM to μC
Grzegorz Mazur, Institute of Computer Science, Nowowiejska, Poland

The code in Listing 1 provides the interface between any MCS-51 family of μCs and a 24C01a/2/4/8/16 I2C EEPROM. The interface is purely software-driven, so any μC port pins can control the EEPROM. This code is approximately two times smaller and approximately 20% faster than similar routines published by Atmel Corp (www.atmel.com). Careful coding of low-level routines and structural optimization produce the performance improvements.

The code is tuned for a -51 running at 12 MHz, but you can also use it at lower clock speeds. For higher speeds, you must adjust low-level routines by inserting "nop" instructions to match I2C-specified timings. The maximum data rate while reading memory content as 16-byte blocks is as high as 8.1 kbytes/sec. With minor modifications, you can use the routines to interface any I2C slave device to a -51 μC.

Listing 1 is available for downloading from EDN’s Web site, www.ednmag.com. At the registered-user area, go into the “Software Center” to download the file from DI-SIG, #2329. (DI #2329).

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**LISTING 1—I2C EEPROM-μC-INTERFACE ROUTINE**

```
DEVRAM equ 06h ; EEPROM I2C device address
scl bit p3.4
sda bit p3.5
; register usage
r0 Out_ptr ; pointer to internal RAM buffer for block transfers
r1 count ; byte count for block transfers
r2 addr_to ; 2-byte memory address (up to 11 bits used)
r3 addr_hi ;
r4 scratch ; used internally

write_block: ; write block from RAM to EEPROM
  t0 fin
  whlop:
  mov a, r0
  inc r0
  call shift_out
  jnz
  djyns r1, whlop
  sjmp stop

write_byte: ; write single byte from ACC to EEPROM
  push acc
  call send_full_address
  pop acc
  jcz
  call shift_out
  djyns stop

read_block: ; read block from EEPROM to RAM
  t0 fin
  call send_full_address
  jcz
  call send_device_addr
  jnc
  call shift_out
  djyns stop

whlop:
  mov a, #0f
  inc r0
  call shift_to
  inc r0
  jmp wait_read

read_random: ; read random byte from EEPROM to ACC
  t0 fin
  call send_full_address
  jcz
  call send_device_addr
  jnc
  call shift_to
  jmp wait_read

read_current: ; read next byte from active EEPROM page to ACC
  t0 fin
  call shift_to
  jmp wait_read

Send: ; Send STOP
  t0 fin
  sjmp stop

stop: ; Send STOP
  t0 fin
  sjmp stop

end
```

**To Vote For This Design, Circle No. 398**
Most object-sensing systems have problems detecting the presence of an object. The system in Figure 1 uses an oscillator to ease detection problems and allow sorting. The oscillator reduces power dissipation in the photodiode by operating the diode at 50% duty cycle. The oscillator also enables a 50% increase in the noise-filter time constant, and it functions as a time-base to allow object sorting. The oscillator chops the photodiode’s bias. The signal the photodetector receives is a square wave; thus, a filter can remove optical noise. You normally need filtering when light shines through fans onto the optical detector. When required, you can place a bandpass filter in series with Q3’s output.

The oscillator frequency has two limits: the response time of the phototransistor and the accuracy of the object-sensing system. Q3 and Q4 are connected in a cascode configuration to minimize the Miller effect in Q4. This connection reduces the pair’s optical transient response to nanoseconds, thus allowing oscillator periods of submicroseconds. Objects on a conveyor belt travel at relatively low speeds. You can calculate their expected time in front of the photodetector, \( t \), from \( t = \frac{d}{s} \), where \( s \) is the conveyor speed in feet per second and \( d \) is the object width in feet.

An object 2 in. long with a belt speed of 3.5 ft/sec blocks the detector for 47.6 msec. If the oscillator period is 250 \( \mu \)sec, the object blocks the detector for approximately 200 periods, so each period equates to 0.5% length accuracy. The system senses two objects—one 2 in. long and one much longer—so 0.5% accuracy is more than adequate. When the detector is unblocked, the inverting input of IC1 is dominant, and it keeps the output of IC1 low. The low state prevents the oscillator’s output from reaching the counter (IC3). Blocking the detector allows \( C_i \) to charge to 5V through \( R_6 \), and the noninverting input of IC1 becomes dominant, starting the count. When the detector is unblocked, the one-shot comprising \( R_{11}, C_5 \), and IC4A pulses IC2B with an end-of-object pulse. The one-shot’s trailing edge triggers the counter-reset one-shot comprising \( R_9, C_6 \), and IC4C.

\( C_i \) and \( R_5 \) form a nuisance filter that rejects short optical noise. The timing is such to enable a 2-in. object to clear the detector while both \( Q_6 \) and \( Q_8 \) are high. When the end-of-object pulse coincides with \( Q_6 \) high, \( Q_7 \) high, and \( Q_8 \) low, the output of IC2B indicates a 2-in. object. This situation is the only time window that can indicate a 2-in. object. If the object is longer than 2 in., \( Q_6 \) goes high, indicating a large object. When the object clears the detector, the reset one-shot resets the counter for another cycle, and \( Q_8 \) quickly discharges \( C_i \) in preparation for another cycle. With the component values shown, the system can sense and discriminate between objects as short as 2 in., separated by 0.1 in. (DI #2325).

An oscillator circuit allows a photodetector to both count and sort objects according to size.
Single-button lock provides high security
Maxwell Strange, Fulton, MD

Figure 1 is the block diagram of an easily programmed, single-button combination lock. You operate the lock by using a series of short and long pulses from a momentary switch that masquerades as a doorbell button. The circuit uses inexpensive CMOS logic. The retriggerable timer, T₂, locks out entries made after the T₁ code-entry window, thereby greatly enhancing security. The circuit in Figure 2 operates as follows: The Schmitt-trigger quad NAND gate, IC₁, debounces the code-entry switch and, with the aid of simple analog circuitry, produces separate outputs for activation times of less than and more than 0.3 sec. These outputs connect to the select gate, IC₅. The initial entry also sets timer T₁ to enable the decoded decade counter, IC₃. Each entry clocks IC₃.

As IC₃ steps through its counts, certain of its output positions represent “short” and connect to IC₅’s inputs; unconnected lines represent “long” positions. This coding arrangement sets the combination. Short pulse positions change the address of IC₅ to select the short input pulse; otherwise, IC₅ selects the long pulse input. The short and long inputs, if present in the programmed sequence, produce an output from IC₅. IC₆ counts the outputs and produces an unlock command only if it counts all pulses. The power-on-reset circuit ensures that no compromise of security arises under any conditions after a power outage. The timers are crucial to the high security of the system. You must enter the code within the 8-sec T₁ window. If you make a mistake, you must wait at least 10 sec for T₂ to time out before you make another attempt. If entries occur continuously and less than 10 sec apart, as an intruder might try, T₂ continuously inhibits counter IC₅.

The lock proves to be reliable over several years of use. The circuit in Figure 2 uses an eight-character combination, which you can quickly enter. A short pulse is a quick jab to the button; a long pulse is only slightly longer. A shorter se-
quence would also be secure; you can implement a shorter code by simply taking the unlock pulse from a lower count on IC6. IC6’s output returns low after 10 sec when T2 resets. If desired, you can generate a lock command, which need not be secure, by adding the simple circuit in Figure 3. (DI #2327).

You can generate a lock command with this additional circuit by rapidly entering four or more short pulses.

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You program your combination by hard-wiring the IC3-IC4 output-to-input connections, LLSSLSSL, where L and S are long and short inputs, respectively, in this example.
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