Lithography for sub-20-nm processes

The recent San Francisco Bay Area Council IEEE Nanotechnology conference addressed the issue of nanoelectronics for sub-20-nm processes. The speakers—from Applied Materials, TSMC (Taiwan Semiconductor Manufacturing Co), Global Foundries, and Tabula—focused on a number of key challenges for tackling production on sub-20-nm designs. These challenges include lithography, materials, new devices, design architectures for interconnect, and 3-D chip stacking. The overriding challenge is lithography, which is the key to creating features at small device sizes.

Lithography has been facing continued throughput and resolution issues since the emergence of the 180-nm node. The current imaging equipment uses a laser light source that has a wavelength of 193 nm—the state of the art for stability and power for more than a decade. The only tool-based enhancement for the main optical path involved the change from dry optics, with air as the transmission medium, to immersion printing, which has a different index of refraction, sending the light beam through a liquid. The wavelength of 193 nm means that simple projection onto a surface can pattern objects larger than the wavelength, and they will appear correct in shape and detail. The next-generation light source, EUV (extreme ultraviolet), features a laser with a wavelength of 13.5 nm (see a related figure at www.edn.com/110106nanotech).

To address features smaller than 13.5 nm, you must use interference patterns and other optical structures to help resolve the objects. These techniques include OPC (optical proximity correction) and SRAF (subresolution-assist-feature) creation and computational scaling of the lithographic source. The key is to reduce the k1 factor in the minimum patterned pitch equation. Computational co-optimization methods include source optimization, focus scatter, mask-optimization software, and dose optimization. These computational approaches have allowed designers to reach the 40-nm node but are not sufficient to push to the next process stages.

New techniques, such as double, triple, and quadruple patterning, have shown positive results for creating the smaller geometries using available technologies. Double patterning is a standard method of printing for current 32/28-nm designs, and manufacturers have developed new equipment to help production facilities maintain their wafer throughput at levels comparable with those of single-patterning machines (Figure 1). To achieve even finer patterns, manufacturers use double patterning twice to create a quadrupling of structures.

EUV starts with a 13.5-nm light source and direct patterning. Using EUV with multiple patterning techniques would allow for high-quality patterning of the original image without the line-edge roughness. A major drawback, however, is that EUV must improve per-hour wafer throughput by at least a factor of 10 to keep up with the equipment in today's fabs.

Self-assembly, which targets use in sub-10-nm processes, suffers from the inability to create the self-assembly in complex patterns. For these applications, the leading technology employs the double-patterning technique using an EUV source. Another alternative uses a direct-write e-beam. To get the throughput, e-beam systems are shifting to the use of multi-beam systems—the approach of choice for high-end ASICs, which may have as many as 10,000 simultaneous beams writing one wafer.

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