Using CMOS gates to generate pulses sometimes causes timing uncertainty due to gate-threshold variations. For accurate pulse widths, you can use BJTs (bipolar-junction transistors). Basing the design on current comparison allows the circuits to operate at low voltages. Proper clamping of the timing capacitor avoids pulse shortening with increased repetition frequency. These circuits work with somewhat less accuracy at supply voltages lower than 5 V.

The heart of this design is a current mirror using modern dual transistors. Process improvements have made many ordinary dual transistors inherently well-matched. Testing a statistically significant sample of PMBT856 devices typically yields a better-than-1-mV match and no mismatches at voltages greater than 2 mV. As has been true for decades, PNP-transistor pairs are better matched than NPN transistors. Testing PMBT3904 devices yields 2-mV matches, with none worse than 3 mV. The packages measure approximately 2 mm on a side, which gives good thermal coupling between the pair. A current mirror with devices having 2-mV mismatch has 8% error. Devices with 3-mV mismatch yield 12% current error. Even with these errors, the circuit makes pulses that are more predictable than those that CMOS devices make.

Figure 1 depicts a simple implementation of a current-mirror pulse generator. It provides good performance over a 0 to 100°C temperature range (Figure 2). The closely spaced traces in the waveforms of these circuits are the 0 and 100°C outputs. Source V2 produces a 40-kHz square wave with a 33% duty cycle. The negative transition of this wave produces a peak current of 4 mA in timing capacitor C1. A time constant of 4.7 μsec is set with the value of resistor R1. The timing current of C1 and R1 passes through diode-connected
transistor Q1, which, being connected in parallel with the base-emitter junction of Q2, forms a current mirror that replicates in Q2 the timing current in C1 and R1. Because the base-to-emitter-voltage-to-emitter-current curves of Q1 and Q2 match and Q1 and Q2 are at the same temperature, Q2 current matches Q1 current. A quiescent current of about 0.85 mA is set in R3. When the timing pulse increases Q2’s current to exceed R3’s quiescent current, Q3 lacks base current and turns off, initiating a negative pulse across load resistor R4. When the timing current decays below the quiescent current of R3, base current flows into Q3, turning it on and terminating the pulse on R4. Q2 saturates early in this pulse and becomes less saturated as the timing current decays.

When V2 transitions positive, it drives the bulk of its current into D1, yielding a short recovery time constant. D1 ceases to conduct at one diode drop above V1’s supply voltage, so the recovery tail from that diode drop to the quiescent base voltage of Q1 depends on the current decay in R1, which is a longer time constant. This simple circuit is stable, varying less than 4% over 100°C. Although stable, this circuit does not provide high-speed operation. In the circuit’s quiescent state, there is no current in either Q1 or Q2, making for a low gain bandwidth. Also, Q3 is in saturation, delaying the initial fall of the pulse across R4 because the free carriers must leave the base region. Q2 also saturates during the pulse, delaying the rise at the end of the pulse.

Figure 3 You can change D1 to a Schottky type to reduce recovery time and add D2 and D3 to keep the transistors out of saturation. R2 biases the current mirror out of the cutoff region.

Figure 5 Replacing D1 with a transistor circuit eliminates the tail-recovery time of the diode.
Because Q₁ and Q₂ are slightly conducting, a voltage one diode drop below that of supply V₁ is always present at their bases.

low that of Figure 1. Changing D₁ to a Schottky diode reduces the recovery-tail voltage that R₁ must dissipate. Add R₂ to draw a keep-alive current of 100 μA through Q₁ and Q₂, speeding turn-on. These keep-alive currents need not affect the timing. You can cancel out their effect with a slight reduction in the value of R₁. Fitting Q₂ and Q₃ with Schottky clamps D₃ and D₄, respectively, keeps the transistors out of saturation. These changes improve high-speed performance (Figure 4).

Although improved, the circuit still relies on D₁ for the final tail of recovery. To eliminate this problem, you can replace D₁ with a fourth transistor, Q₄ (Figure 5). Because transistors Q₂ and Q₃ are slightly conducting, a voltage one diode drop below that of supply V₁ is always present at their bases. You filter this voltage with R₅ and C₂ and provide it as a bias to the base of Q₄. This step keeps Q₄ nearer the threshold of conduction than would a diode to supply V₁. When source V₂ changes to a negative state, Q₄ is fully off and draws no current. When V₂ changes to a positive state, the emitter of Q₄ conducts at voltages above V₁ to catch the recovery transition, further reducing the recovery-tail amplitude.

R₅ may be used to limit Q₄’s base current, but its omission is acceptable if source V₂ has sufficient output resistance. It may be destructive to apply source V₂ swings large enough to cause excess reverse voltage across the Q₄ base-emitter junction. Q₃ and Q₄ can share the same package. These additions further improve the pulse generator’s high-speed performance (Figure 6). EDN

Implement an audio-frequency tilt-equalizer filter

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In the 1970s, Quad Ltd developed a “tilt” audio-tone control, which first appeared on the company’s model 34 preamplifier. The tilt control tilts the frequency content of the audio signal by simultaneously boosting the treble and cutting the bass frequencies, or vice versa (Figure 1). Only one knob is needed to tilt the frequency response around a pivot frequency, Fₚ (Figure 2).

Quad Ltd never published a transfer function for the filter. You need a Spice simulation and many trial-and-error cycles to tune it to your desired response. By deriving the transfer function, you can easily select the component values. Surprisingly, the transfer function also shows how you can make the tilt response asymmetric, with different amounts of boost and cut. You begin deriving the transfer function by expressing the input versus the output as a function of dc-feedback resistor, Rₓ, and Z, the complex impedance of the RC branches:

\[
\frac{V₀}{V₁} = \frac{X×(Z–Rₓ)+Z×(P₁+Rₓ)}{X×(Z–Rₓ)+Z×(Z+P₁)}
\]

where X indicates the wiper position of potentiometer P₁, and the values of the resistors and capacitors define Z:

\[
Z = R + \frac{1}{2×π×F×C}
\]

The frequency response in Figure 2 is for the extreme wiper positions, where X = 0 or P₁. All of the other responses, with 0 less than X and X less than P₁, lie between those curves. To get the frequency responses in decibels, multiply the log of the absolute value of the transfer function by 20: 20log(|TF|). To get a log/log scale on the graph, substitute 10⁰ for F on the X axis. Pivot frequency Fₚ depends on component value, including the setting of potentiometer P₁, as it sweeps between an X value of 0 and P₁, where Rₓ must be greater than R:

\[
Fₚ = \frac{\sqrt{(P₁+2×Rₓ)}}{2×π×C×\sqrt{(Rₓ–R)×(Rₓ–R)+\sqrt{(P₁×(R₁+Rₓ)+2×R×Rₓ)}}}
\]
Figure 2 This frequency response is for the extreme wiper positions, where $X=0$ or $P_1$. All of the other responses, with $0 < X < P_1$, lie between these curves.

Figure 3 $R_f$ is 16.66 kΩ, $R$ is 7.14 kΩ, and $C$ is 12.24 nF.
To calculate component values, you first define the maximum low-boost asymptote as \(M_L\), when the frequency goes to 0 Hz and the potentiometer's value is also 0 \(\Omega\). You then define the maximum high-boost asymptote as \(M_H\), when the input frequency goes to infinity, and set the potentiometer to its maximum value. This step gives the component values for \(R_L\), \(R\), and \(C\):

\[
R_L = \frac{P_1}{M_L-1};
\]

\[
R = \frac{P_1}{M_H-1};
\]

\[
C = \left[\frac{(M_L-1) \times \sqrt{(M_L+1) \times (M_H \times M_L-1)^{3/2}}}\right]
\]

\[
\left(\frac{M_H-1}{(M_L-1) \times (M_H \times M_L-1)}\right)
\]

\[
2 \times \pi \times M_L \times P_1 \times F_P \times (M_H-1) \times \sqrt{(M_H+1)}.
\]

For the equations to work, \(M_L\) and \((M_H \times M_L-1)\) must be greater than 0. You can choose any reasonable value of potentiometer \(P_1\). For example, select a \(P_1\) value of 50 k\(\Omega\), a desired pivot frequency of 1 kHz, a maximum low-frequency boost of 4, and a maximum high-frequency boost of 2. The equations yield an \(R_L\) of 16.66 k\(\Omega\), an \(R\) of 7.14 k\(\Omega\), and a \(C\) of 12.24 n\(\text{F}\) (Figure 3).

You take 20 times the log of \(M_L\) to get the response in decibels, so an \(M_L\) of 4 is the 12-dB maximum low-frequency boost, and an \(M_H\) of 2 represents the 6-dB maximum high-frequency boost. When you normalize the resistor and capacitor values to standard values, you get only a minor error in your desired response. By defining the variables \(M_L\) and \(M_H\), you can make tilt equalizers that have an asymmetric response between boost and attenuation.

![Figure 4](www.edn.com) Voltagess \(V_I\), \(V_O\), and \(V\) are all referred to ground.

### The Goal is to Find \(V_O/V_I\); You Need Not Solve All of the Unknowns.

A detailed derivation of the transfer function is included here. You begin by defining voltages \(V_I\), \(V_O\), and \(V\), all referred to ground (Figure 4). In this case, \(I_1\), \(I_2\), and \(I_P\) are the minimal number of unknown currents. Because an op amp serves the output to keep the input pins at the same voltage, the potentiometer wiper is at 0V, a virtual ground. Further assume the infinite input impedance of the op-amp input pins so that the current at the inverting pin is 0A. \(V_I\) and \(V_O\) are unknown, letting you write a set of equations for the conditions:

\[
V_I = I_1 \times Z+(1+I_1)R_F+V_O
\]

\[
\text{[Loop } V_I \rightarrow Z \text{ (input) } \rightarrow R_F \text{ (output) } \rightarrow V_O]\];

\[
V_I = (1+I_1)R_F+I_1Z+V_O
\]

\[
\text{[Loop } V_I \rightarrow R_F \text{ (input) } \rightarrow Z \text{ (output) } \rightarrow V_O]\];

\[
V_I = (1+I_1)R_F+I_1X+0
\]

\[
\text{[Loop } V_I \rightarrow R_F \text{ (input) } \rightarrow X(P_1, \text{ wiper}) \rightarrow \text{virtual ground}]\]

\[
0 = I_1(P_1-Z)+I_1P+V_O
\]

\[
\text{[Loop virtual ground } \rightarrow P_1 \times X \rightarrow P_F \rightarrow R_F \text{ (output) } \rightarrow V_O];
\]

\[
V_I = (1+I_1)R_F+P+I_1R_F+V_O
\]

\[
\text{[Loop } V_I \rightarrow RF \text{ (input) } \rightarrow P_1 \rightarrow R_F \text{ (output) } \rightarrow V_O]\].

Remember that \(Z\) is the complex impedance of the RC branches. Now rearrange the equations:

\[
V_I = I_1(R_F+Z)+I_1R_F+V_O
\]

\[
V_I = I_1(R_F+Z)+I_1R_F+V_O
\]

\[
V_I = I_1R_F+I_1X(R_F+R_F);
\]

\[
V_I = I_1(R_F+Z)+I_1R_F+V_O
\]

\[
V_I = I_1R_F+I_1P+I_1P+2R_F+V_O
\]

From the first and second equations you can deduce that \(I_1\) equals \(I_1\). You can now substitute into the last three equations and rearrange them to get the final set:

\[
V_I = I_1(R_F+Z)+I_1R_F+V_O
\]

\[
V_I = 2I_1R_F+I_1P+2R_F+V_O
\]

\[
I_1 = (I_1(X-P_1-R_F)-V_O)/(R_F);
\]

\[
V_I = 2I_1R_F+I_1P+2R_F+V_O
\]

The goal is to find \(V_O/V_I\); you need not solve all of the unknowns. If you substitute \(I_1\) from the third equation above into the second equation, you can find \(I_P\). You then substitute \(I_P\) into the fourth equation and find the ratio of \(V_O/V_I\), yielding the first equation in this Design Idea. This result is congruent with the actual numerical value of the examples in Reference 1.EDN

### Reference

The circuit diagrammed in the figure provides a 70-dB automatic-gain-control range for input voltages of −60 to +10 dBm over a bandwidth of 55 Hz to 15 kHz. The worst-case distortion is 3%, but distortion typically measures less than 1% in the 100-Hz to 10-kHz range.

The signal autoranges to keep the input to the AGC section between −60 and −25 dBm; this procedure allows the FET to operate in its most linear region. A comparator performs the autoranging, comparing a −25-dBm reference with the signal from A1 and A2. A4 furnishes the AGC action, settling a −15-dBm output as a reference voltage; A5 provides a fixed 15-dB gain and an output of 0 dBm. A6, A7, and the FET constitute the AGC’s feedback circuit.

Figure 1 A comparator autoranges to ensure that the AGC sees a signal between −60 and −25 dBm, keeping the FET in its linear region.