The CD4011 CMOS NAND gate has a typical input current of 10 pA at room temperature. You can charge a capacitor connected to the gate input with currents on the order of hundreds of picoamperes and neglect the influence of the gate-input current on the charging time of the capacitor. You normally need large-value resistors to limit currents to this low level. These resistors are not commonly available. You can instead use a transistor as a current attenuator, despite its more usual amplifying nature.

The circuit in Figure 1 uses one CD4011 package containing four NAND gates, which you can use to build four independent long-duration timers. Note, however, that temperature variations and component parameters affect the timing, a situation that may be acceptable if you are not concerned about accurate timing and need only a simple circuit without large-value electrolytic capacitors and resistors.

The series-connected diode voltage drops of D1 and D2 bias current source Q1. The resulting voltage across R1 is a Q1 base-to-emitter-voltage junction drop less and sets the Q2 collector current, which is also the Q2 emitter current. The resulting Q2 base current is its emitter current divided by its current gain and charges timing capacitor C1.

Before the start of the timed period, the gate output is high, biasing on Q3 and Q1, allowing C1 to charge through the base-emitter junction of Q2. This action holds the gate input sufficiently below its switching threshold to maintain its high output state. Momentarily closing and then releasing S1 starts the timed period by discharging C1. This action drives the gate output low and ensures that Q3 is biased off, which allows Q2 and Q1 to slowly charge C1 through the constant-current action. The power-supply current draw of the gate increases somewhat as its input voltage pulls away from the 5V rail.

When the C1 charge reaches the gate-switching threshold of approximately 2.5V, the output begins to rise, turning on Q3. This action increases the current through Q2 and Q1, resulting in saturation of Q2 and a faster charging of C1. This positive feedback provides the necessary hysteresis to complete the charging of C1 and return the gate output high.

Linearity with changes in R1 is impossible due to variations in the transistor's current gain. The built and tested circuit does exhibit linearity with the value of timing capacitor C1, which you can choose experimentally for the required time. Once you determine a time for a short interval, such as that for a 10- or a 100-nF capacitor, you can use this knowledge to scale to longer timing. In the tested circuit, with R1 set to 1 MΩ, a C1 value of 10 nF results in a time of 10 sec; a C1 value of 100 nF increases the time to 100 sec.

Editor's notes: Constructing a low-current circuit is challenging. Some types of PCB-soldering flux can become conductive, wreaking havoc with what should be a tiny current. Consider “open-air” connection of the Q1-emitter collector and the Q2-emitter base leads to remove them from the board.

Transistor-leakage currents and current gains vary widely from device to device and with temperature. This variation can drastically affect the expected low-level current and capacitor charge time. Although the CD4011’s typical input current...
is 10 pA at room temperature, it could be as high as 100 nA and increase to 1 μA at high temperature. Likewise, the transistor collector-to-base leakage could be a maximum of 15 nA at room temperature and 125 μA at high temperature, and it approximately doubles for every 10°C rise in temperature. It might be necessary to hand-select transistors and CD4011 inputs or devices to overcome this problem. Also, remember to tie any other unused CD4011-gate inputs to ground or 5V to avoid floating-input problems.

Do not set R1 so low that Q1 or Q2 saturates during the timed period; they must remain in their linear region as set by the value of the Q2 collector resistor. Timing capacitor C1 should have a high-quality, low-leakage dielectric, such as polyester; check the leakage specifications of the size and type you intend to use for suitability with the low-level current.

EDN

Microcontroller drives piezoelectric buzzer at high voltage
Mehmet Efe Ozbek, PhD, Atilim University, Ankara, Turkey

Piezoelectric buzzers find wide use in embedded systems for audible-signal generation. You can drive a piezoelectric element directly from a microcontroller’s I/O pins, but the maximum voltage rating and loudness of a piezoelectric buzzer are typically several times larger than the voltage an I/O pin supplies. Using four enhancement-mode MOSFETs that connect in an H-bridge configuration, the microcontroller can drive the buzzer at a high alternating voltage. The gate terminals of the N-channel transistors in the lower arms of the bridge can connect directly to the microcontroller’s I/O pins. The voltage level on the I/O pins is insufficient for switching the P-channel transistors, however.

The circuit in Figure 1 solves the problem using a cross-coupled configuration. The operation is as follows: The microcontroller turns Q4 on and Q2 off by applying high- and low-logic-level voltages to I/O Pin 1 and I/O Pin 2, respectively. The voltage on Node A goes low, turning on Q3. Node B is now 15V, which is sufficient to keep Q1 off. The voltage on the piezoelectric buzzer is 15V. The microcontroller then toggles I/O Pin 1 and I/O Pin 2, resulting in a piezoelectric voltage of −15V for an effective 30V p-p. These cycles are repeated to generate an alternating voltage with the desired frequency. By using MOSFETs with proper voltage ratings, you can use higher supply voltages that the piezoelectric element can tolerate.

EDN

Circuit simultaneously delivers square and square root of two input voltages
Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

This Design Idea requires inputs in a circuit in a previous Design Idea (Reference 1). IC3 and IC1 are ADG5213 quad switches with individual logic-level control inputs (Figure 1 and Reference 2). With a high input, switches S1 and S2 are open, and switches S3 and S4 are closed. The switches toggle to opposite states with their control inputs low. The circuit is in the idle pretriggered condition. During the initial idle condition before a clock rising-edge trigger, Q is high and, through ICn, holds switches S2 and S1 of IC1 in the open position. Q is low, and, through IC3’s Reset high closes IC3’s S1 and S0, discharging C12 and C14 and zeroing the input voltage to unity-gain amplifiers IC20 and IC21. Q low also sets Track 2 low through IC3 and holds IC3’s S3 and S4 in the open position. The circuit retains any sampled voltages from a previous operation in sample-and-hold capacitors C31 and C32; these voltages appear at VOUTX and VOUTY through unity-gain amplifiers IC2A and IC2B.

Signals VOUTL and VOUTQ from the linear and quadratic pulse generator are at 0V during idle, holding comparator outputs IC3 and IC2 low. A rising trigger edge at the clock signal begins the ramp generation of VOUTX and VOUTQ. The Q and IC2 outputs fall low, closing IC3’s S1 and S0 and ensuring that Track 2 remains low. Q rises and forces Reset low through IC3, opening S1 and S0 of IC1 and allowing C31 to follow the rising VOUTL and C32 to follow the rising VOUTQ.

When linear ramp VOUTL rises to
analog input $V_x$, IC$_4$'s output rises and, through IC$_{8}$, Track 1L opens S$_2$ of IC$_1$ and allows C$_{T2}$ to hold the present level of $V_{OUTQ}$. In a similar manner, when quadratic ramp $V_{OUTQ}$ rises to analog input $V_y$, IC$_5$'s output rises and, through IC$_{8}$, Track 1Q opens IC$_1$'s S$_3$ and allows C$_{T4}$ to hold $V_{OUTL}$'s present level. The pulse generator terminates when the ramps reach 5V. The ramps then fall back to 0V, Q returns high, and Q returns low. The rise of Q immediately triggers IC$_6$ to generate a high pulse of approximately 20 μsec on Track 2 based on RD1 and CD1. This action closes IC$_3$'s S$_1$ and S$_4$, allowing the sampled voltages on C$_{T2}$ and C$_{T4}$ to transfer to C$_{S1}$ and C$_{S2}$ through unity-gain amplifiers IC$_{3B}$ and IC$_{2C}$. Unity-gain amplifiers IC$_{2A}$ and IC$_{2B}$ present the C$_{S1}$ and C$_{S2}$ voltages at $V_{OUTX}$ and $V_{OUTY}$. When Track 2 returns low, IC$_1$'s S$_1$ and S$_3$ open, and the sampled voltages on C$_{S1}$ and C$_{S2}$ are retained.

The fall of Q triggers IC$_7$ to produce a 50-μsec delayed rise on Reset, which RD$_2$ and CD$_2$ time to occur after Track 2 has returned low and the sampled voltages are safely captured on C$_{S1}$ and C$_{S2}$. Reset's high state closes IC$_1$'s S$_1$ and S$_4$, discharging C$_{T2}$ and C$_{T4}$ in preparation for the next trigger. $V_{OUTX}$ is the squared voltage of input $V_x$, and $V_{OUTY}$ is the square root of the voltage of input $V_y$. You can view the equations at www.edn.com/120301dia.EDN

**REFERENCES**


Figure 1 With this circuit, you can find the square at Channel X and the square root at Channel Y for any positive dc or slowly varying voltages of 0 to 5V.
Conversion circuit handles binary or BCD

R Srinivasan, R Ramesh, and DK Murthi, National Aeronautical Lab, Bangalore, India

Systems requiring arithmetic operations on data usually perform those operations in binary form. As a result, they must convert the data to BCD form for display purposes. Address-selection information from digit switches, on the other hand, must be converted to binary form for use in memory-addressing operations.

For applications not requiring fast conversion, a single circuit that can perform both conversions proves adequate. One such circuit (Figure 1) utilizes up/down counters to obtain the desired results. To perform binary-to-BCD conversion, preset the binary value in the binary counter and clear the BCD counter. The binary counter counts down while the BCD counter counts up, and when the binary counter reaches zero, the BCD counter holds.

For BCD-to-binary operation, the BCD counter counts down from the BCD value while the binary counter counts up.

Figure 1 Separate binary and BCD up/down counters permit both binary-to-BCD and BCD-to-binary conversion in one circuit.