extremely close spacing between the power and ground planes can mitigate cavity resonances. Plane capacitance goes up, plane inductance goes down, and plane resistance stays the same, so consequently Q-factor is greatly reduced. This effect becomes especially pronounced when dielectric thickness drops below 1mil. Radiation can also be reduced a lot.

Figure 7.12 shows the via shielding effect at 1GHz frequency. More vias are added in two different ground planes. In comparison with single stitching, four ground via stitching improves planes-to-signal coupling by more than 30%. The insertion loss of the trace is also reduced by half. Although shortening the stitching via distance is more critical than its orientation, the via positioning that is parallel to the shorter plane edge is the preferred orientation for placement.

7.5 Case Study II: DDR2 667 Vref Bus

A case study on the Vref resonance issue of DDR2 667 MT/s bus is described in this section. In the DDR2 platform under this case study, a significant amount of noise was captured on the Vref bus on the DIMM card, as shown in Figure 7.13. On the DDR2 interface, Vref is a reference voltage level generated on the motherboard side and supplied to all SDRAM devices to maintain data signals near their switching level. As the data transfer rate of the DDR interface increases from one generation to another, available voltage margins for data signals decrease significantly. A clean Vref signal has become critical for normal operation of the DDR interface. Moreover, when defining the roadmap for next-generation memory technology, how well local Vref noise is controlled and minimized has become a significant factor.

When the DDR2 interface operated at a 533 MT/s data rate with the worst-case SSO pattern 1010, 143 mV peak-to-peak Vref noise was observed. However, when it operated at the 667 MT/s data rate, 334 mV peak-to-peak Vref noise was observed. In the 533 MT/s case, the noise has a typical SSO appearance, whereas in the 667 MHz case, the noise waveform is much smoother and shows a frequency around 1GHz. It was also observed that the noise level was the highest on device 0, the first device on the DIMM card, and reduced to a lower level on other devices (device 1 to device 8). Three factors have been investigated to identify the root cause: noise source, noise coupling mechanism, and resonance structure. A combination of planar 3D EM simulation and lab VNA measurement was used in this analysis.
7.5 Case Study II: DDR2 667 Vref Bus

7.5.1 Noise Source

Based on the time-domain waveform capture on Figure 7.13, the noise magnitude is dependent on the data switching pattern. The noise has a frequency of 1GHz, the third harmonic of the fundamental data frequency. DDR2 667 MT/s has a fundamental data frequency of 333MHz. It is relatively easy to draw a conclusion that the root cause of the noise is the simultaneous switching output noise of SDRAM buffers in their write cycle on the DIMM card.

7.5.2 Coupling Mechanism

Extensive simulation and measurement data on this case study has shown the SSO noise was coupled from the power and ground planes to the Vref trace due to through-hole vias and reference plane change, as shown in Figure 7.4. Previous work [3] has proved the coupling mechanism between switching noise on power and ground to signal trace analytically and experimentally. For this case study, there are two dominant coupling mechanisms: coupling induced at signal discontinuities due to layer transition and direct SSO coupling. Coupling can be increased due to cavity and signal resonances.
7.5.3 Resonance Structure

The next important consideration is to identify the resonance structure. The magnitude of SSO noise itself is much smaller than the noise observed on the Vref trace. The SSO noise shape is also not as smooth as the Vref noise. Noise magnitude becomes amplified with a certain resonance structure. As illustrated in Figure 7.14, the distributed decoupling scheme was used on the Vref trace design to minimize the capacitor ESL and make the Vref track the midpoint of the signal voltage swing. The standing wave (also called stationary wave) phenomena occurs in all the Vref trace segments between two decoupling capacitors, which form electric walls on both sides, as shown in Figure 7.15. Depending on the physical trace length between the adjacent capacitors and other all inductance components contributing to the electrical length, the structure is subjected to resonance at certain frequencies.

![Resonance structure of the Vref bus](image)

**Figure 7.14** Resonance structure of the Vref bus

In this case, the first device (device 0) has the longest Vref trace routing between the motherboard bypass capacitor to the DIMM bypass capacitor, which should have a relatively low resonance frequency. The other eight devices (devices 1 through 8) have shorter routing between the bypass capacitors, which should have relatively high resonance frequency. According to Figure 7.16, VNA measurements of return loss $S_{11}$ and input impedance $Z_{11}$ at Vref pins show that the resonance frequency at device 0 is around 1.1GHz, and device 7 and device 3 around 1.4 to 1.5 GHz.

**Figure 7.15**  Resonance structure of the Vref bus

![Resonance structure of the Vref bus](image)

**Figure 7.16**  VNA measurements of $S_{11}$ and $Z_{11}$ indicate resonance frequencies at different device locations

This data explains the reason why the 667 MT/s data rate leads to a higher noise level and why the device 0 location has a much higher noise level. First, at the data rate of 667 MT/s, the base frequency is 333MHz and the third harmonics is 1GHz, extremely close to the resonance frequency of Vref trace, whereas at 533 MT/s, the third harmonics of the base frequency is only 800MHz. Second, the device 0 location has the lowest resonance frequency because it has the longest trace length between the bypass capacitors. In short, the analysis shows the root cause of this Vref noise issue as the third harmonic resonance of data signals when DRAM devices are in write mode.

7.5.4 Proposed Solutions
After identifying the root cause of the Vref noise issue, we propose a set of solutions. Three options exist for resolving the problem: eliminating the noise capturing path with SSO noise reduction (which is a separate topic), changing the resonance structure, and adding on-die or off-die filters.

The majority of the solutions have been verified with planar 3D EM time-domain and frequency-domain simulations, which share the same electrical models. Due to many unknown parameters, such as the actual capacitor ESL, DRAM on-die model, and so on, building an accurate baseline planar 3D EM model proved to be a challenging task. Lab VNA measurements were used extensively to calibrate the simulation model at different device locations. Good correlations between simulation and lab measurements were established under two different conditions. This effort was later recognized as the key step for this case study. Figure 7.16 and Figure 7.17 show good correlations between the simulated and measured S_{11} parameter under a base condition. Figure 7.18 and Figure 7.19 show good correlations between simulation and measured S_{11} when an additional bypass capacitor was added at the edge finger location near the DIMM connector. Note that adding an additional bypass capacitor affects only the resonance frequency of device 0 and has virtually no impact on other devices (device 1 through 8). This confirms the analysis on the resonance structure in the previous section.

To minimize the noise coupling due to transition vias, the same reference plane (either power or ground plane) needs to be maintained along the Vref trace, including both motherboard and DIMM segments. In addition, the number of transition vias going through the power and ground planes should be reduced as much as possible.
Figure 7.17  Simulated $S_{11}$ parameters on Vref trace at devices 0, 3, and 7 under base conditions

Figure 7.18  Simulated $S_{11}$ parameters on Vref trace at devices 0, 3, and 7 after adding a bypass capacitor at edge finger location
Figure 7.19  Measured $S_{11}$ parameters on Vref trace at devices 0, 3, and 7 after adding a decoupling capacitor at edge finger location

To change the resonance structure, additional bypass capacitors need to be added to shift the resonance frequency higher, especially at the first device location where the Vref trace is longer. In general, the Vref trace needs to be routed as short as possible to shift the resonance frequency higher. The reduction of the return path will also help change the resonance frequency. More decoupling capacitors (power-to-ground) and stitching vias (power-to-power and ground-to-ground) are required to improve the return path and reduce the electrical length of the Vref trace. The effectiveness of the decoupling capacitor reduces as frequency goes higher, due to ESL and mounting inductance. At higher frequencies, stitching vias are preferred over decoupling capacitors. The simulation also shows that adding an additional Vref trace segment and a bypass capacitor after the end device can help alleviate the noise at the last device, as shown in Figure 7.20. It adds a T-junction to the end device, which appears at all other device locations and reduces noise level due to energy splitting.

With these changes, planar 3D EM simulations based on the models, which correlate to the lab VNA measurements, have demonstrated 62%~87% reduction of noise on the Vref trace, as shown in Figure 7.21 and Figure 7.22.

Figure 7.20  Additional Vref trace segment added at the end device location
Figure 7.21  Time-domain simulation of Vref noise with original board layout

Figure 7.22  Time-domain simulation of Vref noise after eliminating reference plane change, adding an additional stub at end device, and adding a decoupling capacitor at connector pin location
Some additional solutions have also been proposed. An on-die RC low-pass filter can be used to minimize the local Vref noise at a pad location. A series resistor of around 100Ohms can be used. Either a couple hundred pF pull-up and pull-down capacitors or only one pull-down capacitor can be used, as shown in Figure 7.23. The planar 3D frequency domain simulation shows that the pad location is isolated from the Vref noise on the board by adding an on-die filter. Specific R and C values should be determined, based on the value of the existing decoupling capacitor between the power and ground. If the power and ground noises are in phase, both pull-up and pull-down caps are required. If the power and ground noises are 180 degree out of phase, only a pull-down cap is required.

![Figure 7.23 On-die filters for Vref signal](source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.)

If an on-die filter is not available, or a clean Vref signal is desired on board to reduce its impact on other signal traces, an off-die RC low-pass filter or stepped-impedance transmission line low-pass filter can be used. Figure 7.24 shows the idea of using a stepped-impedance transmission line low-pass filter for Vref routing. The signal trace can be routed by connecting wide (low $Z_0$) and narrow (high $Z_0$) segments repetitively. Equivalent to a low-pass LC network, the stepped-impedance structure can help eliminate high-frequency noise and increase isolation between devices on Vref signal.

![Figure 7.24 Off-die stepped impedance filters for Vref signal](source: W. H. Ryu and M. Wang, “A Co-design Methodology of Signal Integrity and Power Integrity,” DesignCon 2006.)
 Appropriately designed on-die and off-die RC or LC low-pass filters will remove high-frequency noise from a Vref signal. On-die filters remove high frequency noise at the pad location, whereas off-die filters remove noise on the trace.

We emphasize that as frequency increases, DIMM geometric dimensions and between-device distance become a significant fraction of a wavelength, which makes a Vref trace more vulnerable to the SSO noise resonance and Vref noise control more challenging. The use of distributed decoupling capacitors will not be sufficient for a higher data rate DDR interface.

Understanding combined signal-power integrity issues in the era of giga-hertz data rates requires an advanced co-design methodology for signal integrity and power integrity analysis. This section has explored a robust co-design methodology with two case studies, namely DDR2-800 control bus and DDR2-667 Vref bus resonance. With the proposed co-design methodology, the complicated power induced resonance problems have been root-caused and consequently, cost-effective solutions, and design guidelines have been identified for the presilicon design stage. Similar principles of signal/power integrity co-analysis can be applied to higher data rate memory devices.

### 7.6 Referencing/Stitching/Decoupling Effects–Single-Ended Interface

Platform stitching vias and decoupling capacitors; also called stitching decoupling capacitors, are used when a critical signal transitions between reference planes. The stitching decoupling capacitors are then connected between the power and ground planes near the critical trace effectively tying the two planes together. The stitching decoupling capacitors have been proved to be critical design components for a single-ended interface to facilitate the return current path and minimize noise coupling from the power plane to signal trace. A simpler or better functionality can be obtained by ground-to-ground and power-to-power stitching via [6, 8]. Figure 7.25 shows the maximum voltage transfer ratios from the plane-to-signal trace with various stitching via distances. The maximum voltage transfer ratio has been extracted up to 5GHz based on full-wave 3D electromagnetic simulation. This demonstrates the significance of stitching vias for high-speed single-ended buses and that the tightened stitching distance rule is required for the multi-GHz interfaces. As high-speed interfaces are adopted more often, a link-level impact assessment and design guidelines for the plane stitching vias and decoupling capacitors are highly desirable for SI engineers and platform designers. Looser stitching/decoupling requirement means spacious board routing, lower cost, and reduced design effort, but its exact indication on platform signal integrity design is unclear. This section attempts to address this question.