The circuit in this Design Idea uses an intrinsic property of collector voltages in one-transformer push-pull dc/dc converters: They have a swing of twice the supply voltage. When you implement these circuits with an NPN device, the collector swings from 0V to twice the supply-rail voltage. When you use PNP devices, the collector voltage swings from VCC to an equal amplitude but negative VCC (Reference 1). In this circuit, a complementary pair of transistors, simultaneously implementing a voltage doubler and a negative-voltage source, drives the two windings of the transformer.

One of the windings of transformer $T_1$ connects to ground, driven by PNP transistor $Q_1$ from VCC (Figure 1). The other winding of $T_1$ connects to $V_{CC}$, and NPN transistor $Q_3$ drives the lower end to ground. $Q_1$ and $Q_3$ drive $Q_2$ and $Q_4$, respectively. The collectors of $Q_1$ and $Q_3$, through resistors $R_4$ and $R_3$, provide cross-coupled drives to $Q_2$ and $Q_4$. $R_1$ and $R_2$ form the collector loads for $Q_2$ and $Q_4$. $D_1$ and $D_3$ prevent the reverse breakdown of $Q_1$ and $Q_3$. The drive configuration and the transformer's winding polarity provide regenerative feedback and self-oscillation so that the transformer alternates between positive and negative saturation, inducing voltages to drive transistors $Q_1$ and $Q_3$ alternately on and off.

A square wave with an amplitude twice $V_{CC}$ is generated at the collector of $Q_1$, which swings nominally from $V_{CC}$ to the equal but negative output voltage. Simultaneously, a square wave with an amplitude twice the supply-rail voltage is generated at the collector of $Q_3$, which swings nominally from 0V to twice the supply-rail voltage. $D_2$ and $C_2$ provide half-wave rectification and filtering of the $Q_1$ collector waveform generating the negative voltage output. Half-wave rectification and filtering of the $Q_3$ collector waveform using $D_4$ and $C_4$ generate the doubler's output.

$T_1$ is 200 turns of bifilar AWG 37 enameled wire.
You can use an LED as a photoelectric sensor. A previous Design Idea shows that such a switch is highly power-efficient, consuming almost no power (Reference 1). However, you cannot adjust that configuration to switch at the desired light intensity. You can adjust the circuit in this Design Idea to any threshold level of light intensity necessary to maintain the on state of the photoelectric switch while retaining almost the same power efficiency of the original circuit (Figure 1).

Illuminating the reverse-biased green LED with ambient light causes the small current that flows through the LED to form the base current of the BC549 NPN transistor, which is amplified and passed on to the base of the BC177 PNP transistor. A magnified version of this current flows through the emitter of the BC177. The voltage drop across the emitter resistor depends on its value and the current flowing through it, which in turn determines the voltage drop across the CE terminals of the BC549.

By adjusting the value of the series emitter resistor you can set a voltage corresponding to logic zero of a CMOS gate for any desired intensity of light falling on the green LED. This intensity depends heavily on the response of the green LED and the current gains of the two transistors, so you select the resistor value by shorting out combinations of the series string of resistors and use the 10-MΩ potentiometer as a fine adjustment. Once you find a suitable value,
you can remove the unused resistors from your circuit.

When the ambient light intensity falls below this level, both the base current of the BC549 and the current through the emitter series resistors decrease. This decrease raises the input voltage at the CD4011 logic gate higher than the CMOS switching threshold. The typical gate sourcing current at a 3V output is approximately 3 to 4 mA per gate; running three gates in parallel delivers approximately 10 mA to the white LED. You can use inverting or noninverting gates for the same result. The circuit still retains its power efficiency because the required series-resistor values normally exceed 10 MΩ.

You can check a green LED's suitability for use as a photodiode by measuring the voltage drop across the LED with a 200-mV digital multimeter. If the LED is suitable as a photoelectric sensor, you will see a voltage of 0.3 to 1 mV across it, and this voltage changes with the intensity of light falling on the LED.

REFERENCE

Obtain a gain of 450 from one vacuum tube
Lyle Russell Williams, St Charles, MO

A direct-conversion radio receiver required an audio gain of 450 from a pentode vacuum tube. A pentode has a high transconductance—that is, the ratio of the change in plate current to the change of the control grid voltage that caused it. To get high gain, however, it needs a high load impedance. RF applications with pentodes often used LC-tuned circuits in their plate loads in which the impedance at resonance and, therefore, the gain is high. It is typically impossible to implement a high load impedance using an untuned circuit because of the dc requirements of the tube.

RF APPLICATIONS WITH PENTODES OFTEN USED LC-TUNED CIRCUITS IN THEIR PLATE LOADS.

For instance, a 6AU6 pentode vacuum tube needs a quiescent plate current of approximately 5 mA (Figure 1). If the quiescent dc plate voltage is to be 60V, the load resistance must be no more than 12 kΩ. The 0.5-MΩ plate resistance of the tube and the 1-MΩ load of the next stage are negligible with respect to the 12-kΩ load. With a transconductance of 3900 siemens, those requirements demand an audio gain of 45. You can easily achieve this gain with a triode tube.

To get a high load impedance with an untuned plate circuit, you can use a transistor current source for the tube (Figure 2). The transistor has no gain but functions as an active load for the tube and supplies the 5-mA plate current. You adjust the 500Ω potentiometer to obtain 60V dc at the plate. The gain of the circuit is approximately 450. This gain implies a 150-kΩ load impedance that the transistor supplies in parallel with the plate resistance and the resistance of the next stage. Alternatively, you can use two triode tube circuits in series, each having a gain of 21.

Figure 1 A 6AU6 pentode vacuum tube needs a quiescent plate current of approximately 5 mA.

Figure 2 To get a high load impedance with an untuned plate circuit, you can use a transistor current source for the tube.
This Design Idea describes a simple yet powerful handheld probe that you can use as both a logic probe and a pulse generator either individually or simultaneously. This feature makes the probe useful for testing DIP digital ICs, such as gates, flip-flops, and counters, using a socketed fixture with three-post jumpers to connect each pin to logic high or logic low or to 5V or ground. Three pushbutton switches, two dual-color LEDs, and two probe tips are built into a plastic cylinder, such as an empty 20g-or-larger glue-stick tube. The generator’s probe tip hooks to fit onto the test fixture’s jumper pins and mounts onto a spring, such as those in retractor ball-point pens, for flexibility, and it allows the logic-probe tip to move to the output under test. Two of the pushbutton switches set the generator’s quiescent state for a high output or a low output. The third switch briefly single-pulses the output to the opposite state. If the switch is pressed for longer than 2 seconds, the output produces a pulse train.

IC\textsubscript{1A}, an NE556, is a 2-sec monostable circuit, which triggers a 1-msec pulse-generator circuit employing gate G\textsubscript{1}, resistor R\textsubscript{1}, and capacitor C\textsubscript{1} (Figure 1a). G\textsubscript{3} buffers the circuit. The output of the monostable circuit also passes through G\textsubscript{2} and G\textsubscript{3} to mask the output of the astable component, IC\textsubscript{1B}, an NE556 that provides the pulse train. To prevent any spurious pulse from reaching output Probe A when switch S\textsubscript{1} is not depressed, keep IC\textsubscript{1B} deactivated by applying a low voltage to its reset Pin 4 through transistor Q\textsubscript{1}, whose biasing a 0.68-μF capacitor further guards.

When you press switch S\textsubscript{1} for a short Probing system lets you test digital ICs
Raju Baddi, Tata Institute of Fundamental Research, Pune, India

Figure 1 This circuit combines analog and digital functions. Probe A is the pulse-generator probe, and probe B is the logic probe (a). Although not shown, a 100-μF capacitor should be connected between the supply and ground. Red LEDs indicate logic zero, and green LEDs display logic one (b).
time, IC\textsubscript{1A} fires and produces a high output for approximately 2 sec. The 1-msec pulse from G\textsubscript{1}, R\textsubscript{1}, C\textsubscript{1}, and G\textsubscript{4} reaches the pulse Probe A through the XOR function comprising G\textsubscript{5} through G\textsubscript{8}, and the output of the astable IC\textsubscript{1B} is masked at G\textsubscript{3} from reaching the XOR. If you depress switch S\textsubscript{1} for longer than 2 sec, the monostable IC\textsubscript{1A} times out. This action unMASKS G\textsubscript{3} and allows the 70-Hz oscillation from IC\textsubscript{1B} to reach the XOR. G\textsubscript{9} and G\textsubscript{10} form a bistable circuit, which “remembers” the most recently pressed S\textsubscript{2} or S\textsubscript{3} switch and controls the inverting and noninverting operation of the XOR function. G\textsubscript{3} and G\textsubscript{4} together drive the dual-color LED to indicate the pulse generator’s polarity. Red indicates that Probe A’s output is mainly logic zero, with the single 1-msec pulse a logic high. Green indicates the opposite.

The LM358 acts as a window-detector logic probe (Figure 1b). With the values in the figure, the red LED lights at Probe B voltages of less than 35% of the supply voltage, and the green LED lights at voltages greater than 65% of the supply voltage. Neither LED lights between these voltages. You may wish to adjust the resistor network to reduce the lower threshold to include the transistor-transistor-logic zero of less than 0.8V.

If you use CD4011 quad NAND gates, you can externally power the probe at 4.5 to 15V. Using a CD4093 Schmitt-trigger quad NAND for G\textsubscript{3} through G\textsubscript{4} ensures no spurious oscillations as a result of the slow voltage rise at timing capacitor C\textsubscript{1}. If your design requires a higher-current generator drive, you can add a pair of NPN and PNP boost transistors to the output.

**Figure 2** Program this test jig with header posts and jumpers for the IC under test.

**Figure 3** To inject a signal, hook the flexible spring-mounted generator, Probe A, onto the appropriate input post and then move logic Probe B to the corresponding output post or pin.

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**REFERENCES**