Automated test equipment is becoming a yield-metrology tool that works in conjunction with yield-analysis software.

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As advances in IC technology have resulted in geometry and process variations, manufacturers have encountered a drop in both initial and mature yield and an increase in yield ramp-up time. Systematic design-process interactions are now the dominant yield-loss mechanisms, and their effect is exaggerated by design complexity. Manufacturers can address the new yield-loss mechanisms by using a combination of automatic test equipment (ATE) and design-for-test (DFT) software to capture and analyze defects during high-volume production and reduce process problems on the manufacturing line.

The new role of production testing
The use of scan-based test structures has become prevalent in DFT applications. In addition to using at-speed test to check for stuck-at faults, manufacturers can use the technique to find timing-related defects in nanometer technologies. Also, newer fault models such as bridge (Ref. 1), N-detection (Ref. 2), false-multicycle (Ref. 3), and small-delay-defect (Ref. 4) along with new pattern-generation tools make it possible for manufacturers to detect defects in sub-90-nm designs.

The increased challenges of yield management at the submicron level have resulted in a new role for ATE. Previously, ATE was limited to applying tests to perform a simple quality screen, and testers collected only pass/fail statistics. Now, manufacturers are finding that newer, flexible ATE systems can collect failure data on the scan cell nodes inside a chip (Figure 1) and provide that data to diagnosis tools, which in turn can perform defect analysis that leads to process and design improvements (Figure 2). Essentially, the ATE becomes a yield-metrology tool as well as a quality-screen tool.

Defect diagnosis roughly consists of two phases. In the first, engineers must analyze a sufficient number of failed die to identify a failure trend. In the second, they must select a group of die that may represent the failure trend and perform further analysis, which may include refined diagnosis and linking to physical layout data followed by physical failure analysis. The goal is to find the defect location, identify the failure mechanism, and characterize the failure behavior.

Failure diagnosis data requirements
An ATE system that will be used in a failure-diagnosis and yield-improvement process must collect the following sub-die-level data:

- Voltage and current measurements. These traditional measurements remain important and need to be correlated
with other sub-die-level measurements during statistical analysis.

- **Digital test results from (compressed) scan/BIST test patterns.** The logic-diagnosis software needs to know the exact position of a fail bit from the scan chain in order to identify the root cause.

- **Memory test results from built-in self-test or built-in self-repair (BIST/BISR).** Information from BIST/BISR is required for monitoring silicon processes and optimizing redundancy schemes.

The fact that the above data needs to be collected during high-volume manufacturing test puts additional demands on the ATE’s performance. In particular, the following conditions must be satisfied by the ATE to make volume diagnosis viable:

- **Low test-time impact.** The data collection time for volume diagnosis typically must be less than 5% of the device test time.

- **Low data volume.** The data volume typically must be kept to about 5 kbytes per device without compromising diagnosis capability, leading to the need for intelligent data collection.

- **Efficient data flow.** The system should be able to support the diagnosis of more than 100,000 faulty devices per day.

**Diagnosis software requirements**

Scan diagnosis is a viable approach for identifying the cause of physical defects. By correlating logic simulation information, physical layout data, and test results from defective devices, diagnosis software can identify a failure site quickly.

After the software determines the first-level correlations, you can take additional steps to isolate the location of a defect. These steps include regenerating scan patterns based on diagnosis results, re-testing, and re-running diagnosis routines. Once you locate a physical defect, you can use traditional physical failure-analysis methods to analyze it more fully.

**Combining hardware and software**

To help customers with their defect-diagnosis and process-improvement programs, our companies integrated the Verigy V93000 SOC (system-on-chip) tester with the Mentor Graphics YieldAssist software tools. Although you could use products from various companies to set up a yield-improvement system, we will explain how such a system can work by describing our setup.

To begin, the ATE system feeds links to information on netlist and test patterns—along with the test results from devices that have failed in production—into the diagnosis software. The software performs some consistency checks on the data to help ensure accuracy and then performs a series of statistical-analysis steps to identify a failure signature and provide for symptom separation, suspect type classification, suspect scoring and ranking, and net, cell, and pin location.

The results are fed into a test debug and logic-visualization tool that identifies the logical location of the failure and into a physical-verification tool that provides a hierarchical visualization of the device’s physical design. By correlating the logical type and location of the failure to the physical location of the failure, the engineer can rapidly determine if the failure is due to a layout “hot spot,” such as interconnects subject to bridging or pinching.

Because scan testing is based on the direct stimulation and response of the actual internal logic (vs. external functional testing), it provides the best information for pinpointing the cause of systematic and random yield loss resulting from manufacturing process variability.

When choosing scan test and diagnosis technology, engineers should look for these capabilities:

- **Low test-time impact.**
- **Low data volume.**
- **Efficient data flow.**

**FIGURE 2.** ATE acquires a diagnostic role when combined with yield-analysis software.

**FIGURE 3.** (a) Typical ATE-to-EDA datalog flows involve custom data formats on a per-tester and per-tool basis. (b) An improved flow employs a standard format.
• capabilities for scan-chain (Ref. 5), logic, and memory diagnosis;
• the ability to handle large volumes of test data and automation of the analysis process;
• support for suspect classification, score, ranking, net name, and pin identification;
• links to physical-verification and design-for-manufacturing (DFM) tools;
• support for a variety of failure file formats to accommodate production testing systems; and
• direct diagnosis from both compressed (Ref. 6) and uncompressed test results.

memory can be used efficiently. Because test is a cost- and time-sensitive operation, the ATE must collect and transfer failure data with minimal impact on throughput. The ATE must address data capture in single- and multiple-device test environments:
• Fail data capture for a single device. This can be measured as fails captured per second. An efficient ATE system will have zero or close-to-zero overhead for the information collection.
• Fail data capture in multisite flows. Multisite testing presents a challenge as well as

An opportunity for yield improvement. On the challenge side, multisite testing adds extra data volume and requires synchronization across sites. On the opportunities side, ATE can take advantage of multisite testing to hide the data collection on the failed dice behind the test time for the passing dice, thus reducing the effects on throughput.

In addition, datalogging efficiency depends on the ATE system being able to support adaptive datalogging and on its being able to provide a fast communication medium to transfer the collected fail data to the diagnosis tools.

As data is transferred from design to test to design, the ATE must provide a means for data integrity and data synchronization. Specifically, the tester needs to
• preserve information on any transformations that take place on any piece of data during the test-program generation as well as during data collection,
• perform data-integrity checks at regular intervals so the downstream analysis tools can ascertain that the data has not changed since the last synchronization point, and
• support standard data formats for multi-tool, multivendor environments.

This last point is important for customers with ATE from multiple vendors on the test floor. Supporting custom formats on a per-ATE and per-tool basis is a tedious process that is prone to errors. Figure 3a shows the complexity of transformations. Ideally, all the ATE and analysis tools should use a standard format, as shown in Figure 3b, for greater efficiency and accuracy.

**Automating volume diagnosis**

Figure 1 shows a volume diagnosis flow for a single design using a single tester. In reality, a single design may have to be tested using multiple testers, and different designs may get tested on one test floor. Figure 4 shows an automated volume scan-diagnosis flow that our companies devised for such a test environment. A diagnosis server session called “monitor” captures failure data from multiple testers assigned to different devices, each with its own working directory. If there are existing failure files in a working directory, the server automatically checks data consistency on the new data.

Once data passes the consistency check, the monitor process distributes work to analyzer processes that perform fault diagnosis. Multiple analyzer processes can be assigned to a device data stream. Each analyzer corresponds to one diagnosis engine. If all failure files have been diagnosed, the server remains in an idle state waiting for new failure files. The results of analysis can be output in standard scan-diagnosis report format, in CSV tables, or potentially in other database formats. The results can be encoded or non-encoded.

Accurate diagnosis depends on input-data-consistency checks, a full simulation of passing and failing patterns, a complete test failure log, and access to physical design (layout) data. Experiments performed with the Mentor software found that compressed pattern diagnosis performs almost as well when compared to diagnosis with uncompressed patterns (Ref. 8). Comparisons of results from compressed and uncompressed patterns

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**FIGURE 4.** The scan-diagnosis automation mode supports multiple designs and multiple testers.

The increasing volume of test patterns required to perform high-quality testing on sub-90-nm ICs has led to widespread adoption of test-pattern compression. Scan test-pattern compression allows high-quality tests to be run while maintaining costs and time to test (Ref. 7). In the context of failure diagnosis, an important issue is whether the compressed patterns can be used for diagnosis without losing important information.

**ATE requirements**

To support the volume diagnosis environment shown in Figure 2, the ATE system must be accurate enough to exhibit low or no self-induced yield loss. In addition, it must support multiple DFT architectures so it can collect the sub-die-level fail information from scan-chain testing, and it should permit selective capture of relevant information from the test process so the available...
show a correlation of 92%, demonstrating the feasibility of a diagnosis flow based on production testing using compressed test patterns.

Advances in technology are demanding a new approach to yield learning using volume diagnosis. Therefore, while various test methods and compression technology are necessary to maintain high-quality and meet low-cost test needs, it is also critical to be able to identify defects quickly and reduce the yield ramp-up process to diagnose a significant volume of failed devices.

The role of ATE is expanding to meet these new requirements of yield improvement, thus closing the loop between DFT and diagnosis. Yield-friendly scan diagnosis can handle large data volumes automatically and efficiently. In addition to pinpointing the location of defects, scan diagnosis provides a learn-failure mechanism through logic simulation and enables physical-layout analysis based on failure data. This will greatly facilitate failure analysis and reduce the yield-learning effort.

REFERENCES


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