A New Method for Receiver Tolerance Testing Using Crest Factor Emulation

Presented by:
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Receiver Tolerance Testing

Receiver tolerance testing probes the ability of a receiver to work with a degraded input signal

Outline

1. Review of tolerance testing
   - The stresses
     • Compliant patterns
     • SJ, ISI, RJ, Noise and SSC
   - And their effects on Receiver components
     • Clock Recovery
     • Equalizer Performance
     • Decision Circuit

2. Difficulties in tolerance testing

3. Crest Factor Emulation and how to test faster, more accurately and at lower expense.
High Speed Serial technology
Trouble from the transmitter

Phase noise $\sim (PLL)^2$
Trouble from the transmission path

- ISI
- Resistance
- Skin effect
- + Dispersion
- Attenuation
- Nonuniform frequency response

Diagram showing a transmitter, backplane, and receiver connected by cables, with a PLL x 60 and a 100 MHz signal from a transmitter.
InterSymbol Interference increases fast with length of channel
InterSymbol Interference increases fast with data rate.

- 3 Gb/s
- 6 Gb/s
The receiver

Distributed clock option

CR BW typ $f_{data}/1667$
Stressed receiver tolerance testing

- Interoperability ➔ meet BER spec with worst case but compliant signal
- BER_{ISI} ~ number of bad trajectories / pattern length
- ISI-caused errors, BER > 10^{-5} typically
- Spec’s: BER < 10^{-12}
Stressed receiver tolerance testing – test pattern

- Interoperability → meet BER spec with worst case but compliant signal
- BER_{ISI} \sim \text{number of bad trajectories / pattern length}
- If ISI causes errors, BER > 10^{-4} typically
- Spec’s: BER < 10^{-12}

Stresses
- Test Pattern
  - Baseline wander
    Mark density = \frac{1}{2}
  - Clock Recovery
    Transition density = \frac{1}{2}
  - ISI
    Trajectories ↔
    Pulse response
Stressed receiver tolerance testing – Deterministic Jitter, DJ

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Stresses
- DJ (aka, BHPJ)
  - ISI
  - SJ and SSC
Stressed receiver tolerance testing – Random Jitter, RJ

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Stresses

- RJ
  - White, Gaussian
  - Reverse-biased diode → Johnson noise
Random Jitter - RJ

- RJ is subtle
  - Smear ISI
  - Probe Rx robustness

- Over 99.7% of RJ effects are < 10% of p-p DJ
  - Lots of tiny stress
  - Outliers are very rare (instance of an outlier)

- Compliance
  BER < 10\(^{-12}\) \(\Rightarrow\) need large Crest Factor
RJ and Crest Factor

The limiting factor in configuring a receiver tolerance test is obtaining an RJ source with sufficient crest factor:

- Otherwise, just use an Arbitrary Waveform Generator
- Crest factor → maximum divergence of distribution from its mean:
  \[
  \text{Crest factor} \equiv \frac{V_{\text{Peak}}}{V_{\text{rms}}} \\
  \text{Gaussian crest factor} = \frac{1}{2} \left( \frac{x_{\text{max}} - x_{\text{min}}}{\sigma} \right)
  \]

- Ideal RJ source has infinite crest factor
  - Unbounded Gaussian
- Real RJ source crest factor increases with run time
RJ and DJ effect on BER vs time-delay (aka Bathtub plot)

- Desire an ideal RJ source: Unbounded Gaussian with white spectrum
  - infinite crest factor
- BER as a function of sampling-point time-delay (aka bathtub plot)
  - CDF of jitter PDF = integral of RJ (DJ pattern)

DJ → inward displacement
RJ → Long smooth tails with structure

Linear scale

Log scale

DJ dominated
Structure and meaning of the stress signal

- Compliance test requires a sig-gen with $14\sigma$ spread in RJ
  - Crest Factor of 7 (8.5 dB)
  - Test at least two freq/amp points on SJ template
  - Measure to a 95% Confidence level

  *Ignoring* that some logic transitions are more stressful than others

  *Need to test over $6\times10^{12}$ bits if there are zero errors*
The problem with random processes: they are random

Remember:

- ISI $\rightarrow$ transition trajectories
- Each trajectory is modified by SJ

What if a large RJ instance occurs on the transition with maximum ISI? **Fail**

What if that large RJ instance occurs on the transition with minimum ISI? **Pass**

Where do we *want* the $7\sigma$ RJ instance to occur to get the most accurate result?

- On the transition of *median* ISI and $\frac{1}{2}$ amplitude SJ
- Truly random fluctuations are **uncontrollable and irreproducable**
  Why would we willingly introduce them in the test lab?

*Random* tests require

- Substantial statistics $\rightarrow$ take a long time
  - BER of $10^{-12} \rightarrow$ many minutes, $10^{-15} \rightarrow$ days, $10^{-18} \rightarrow$ years
Wait.. Why are we doing this?

The goal of stressed receiver tolerance testing:

- Does the receiver tolerate the worst case compliant signal?

... So use the worst case signal ...
Wait.. Why are we doing this?

The goal of stressed receiver tolerance testing:

• Does the receiver tolerate the worst case compliant signal?

… So use the worst case signal …

Why not *just* test here...

and here and here?
Crest Factor Emulation – a better way to make a stressed eye

- In a test lab, you **should** understand the initial conditions of a test

A better way: Apply pseudorandom noise where and when you want it.

Crest Factor Emulation

- Use a deep memory arbitrary waveform generator to synthesize the stressed waveform – including SJ, ISI, SSC, *and* high probability low amplitude RJ
- Introduce low probability, large amplitude instances at $\text{BER} = 10^{-12}$ on those transition(s) to get the most accurate result

Remember:

- The amplitude of 99.7% of RJ instances are < 10% of the DJ p-p value
- A $10^{-12}$ outlier has a displacement of ~ 0.18 UI
Crest Factor Emulation – a better way to apply RJ

Introduction of a low probability, high amplitude instance of jitter by hand is no different than its introduction at random.
- Because it hardly ever happens

• Since the stress signal is prescribed by the standard, there are no surprises at low BERs so...

  just test the high probability DJ regions and the worst case RJ points
Application of Crest Factor Emulation

Median DJ transition

Median DJ transition + $10^{-12}$ RJ outlier
Why Crest Factor Emulation is better

- You put the outlier where it best probes the *actual* $10^{-12}$ BER stress.

- If the RJ outlier occurs on the
  - Worst case ISI trajectory and maximum SJ amplitude then it tests lower than $10^{-12}$
  - Best case ISI trajectory and zero amplitude SJ then it tests greater than $10^{-12}$

  With a truly random signal you never know
  - With Crest Factor emulation you put it in the right place.

- If the receiver **passes** the carefully controlled worst case signal then its BER is assured to be $< 10^{-12}$

- If the receiver **fails**, the failure can be isolated, repeated, and diagnosed
  - Caused by ISI? PJ? RJ?
  - Is it due to baseline wander, clock loss, bad decision circuit?

- **Test time for any BER is reduced to less than a minute**
  - $10^{-12}$, $10^{-15}$, $10^{-18}$ And it’s **not an approximation**
The best way to perform a stressed receiver tolerance test

1. Synthesize the stress pattern with the specified rise/fall time
2. Apply ISI according to the specification
3. Apply SJ with amplitude and frequency prescribed by a template
4. Generate and apply pseudorandom Gaussian RJ to every transition in the signal except the one with median DJ – i.e., the edge with median ISI and ½ amplitude SJ.
5. At this point we have a signal capable of testing every point in the shaded region for the SJ amplitude/frequency we chose in step 3.
6. Apply a single $7\sigma$ displacement to the transition of median DJ displacement.
7. If the receiver tolerates the waveform, return to step 3 and apply another SJ point on the template – repeat once for SJ within the clock recovery bandwidth, once at the end of the roll off, and once above the CR bandwidth.
8. If the receiver fails one of the three tests, find the errored bit(s) in the synthesized waveform and start debugging.
Conclusion: The test lab

The advantages of an AWG-based stress sig-gen:

• Flexibility and ease of use
  – Especially for ISI and de-emphasis

• Control

• Diagnostics

• Speed of test

Thank You!

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Stress 1: The compliant stress pattern

Aggravate baseline wander
- Most receivers are AC coupled
- Vary mark density over times close to the time-constant
e.g., 0010 0010 0010 0010 … 1101 1101 1101 1101

Challenge clock recovery
- CR circuits recover clock from logic transitions in the data
- Vary transition density – long runs of consecutive Identical bits
- Does it lose lock? Does it drift?
  8B/10B encoding limits the run length of CID bits

Intensify Inter-Symbol Interference (ISI)
- Neighboring bits \(\Rightarrow\) average trajectory of logic transitions = ISI
- Need every allowed permutation that extends over the pulse response
Stresses 2 and 3: Sinusoidal Jitter (SJ) and Spread Spectrum Clocking (SSC)

SJ template stresses clock recovery
- Approximate to the clock recovery frequency response

SSC is applied periodic jitter
- Triangle wave, “Hershey’s kiss” FM at ~ 33 kHz
- Spreads radiated energy over frequency band to pass FCC interference regulations
- Clock recovery *must* have sufficient bandwidth to track SSC
Stress 4: Inter-Symbol Interference (ISI)

ISI is the most important stress for today’s serial technologies
- SJ isn’t enough stress to test nonlinear discrete sampling clock recovery circuits
- ISI $\to$ jitter and voltage noise at rational fractions of the data rate

• Expect emerging standards to emphasize ISI
  - Necessary to stress receiver equalization

Equivalent trace lengths
Equivalent cable lengths $\rightarrow$ S-parameter masks

• Hardware intensive sig-gen ISI limited to calibrated backplanes
• AWG-based sig-gen limited by your imagination
Stress 5: Random Jitter (RJ)

RJ
- Gaussian in the time domain
- White frequency spectrum
Stress 5: Random Jitter (RJ) – Stress to BER = 10^{-12}