Test high-speed ADCs for analog-input phase imbalance

Phase imbalance tells you how well a high-speed analog-to-digital converter rejects even-order distortion. Understanding this parameter helps you understand the tradeoffs in designing the analog input network.

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If you use high-speed ADCs (analog-to-digital converters) for product development or you evaluate these devices for use in a design, you must pay attention to the ADC's output harmonics. ADCs typically use differential inputs, which minimizes common-mode noise and distortion, but those inputs work best when they're balanced and symmetrical. You can use a test system consisting of two RF signal generators and an oscilloscope to measure the effects of differential imbalance on an ADC's input.

When an ADC’s differential analog inputs become imbalanced by being driven out of phase, the device’s output will contain increasing even-order harmonics. Using a high-speed ADC, I'll show you how you can measure the ADC's harmonic performance to see the effects of differential imbalance.

Test Setup

The test setup (Figure 1) uses two RF signal generators to drive the ADC's analog inputs at frequencies from 2 MHz to 300 MHz. You must make sure to reference-lock the signal generators to each other. That helps limit unintended phase drift over time. Each signal generator's output passes through a low-pass filter connected to a two-way low-loss splitter. The splitter lets you observe the differential signal with an oscilloscope. You should use low-loss splitters--the same make and model each input. You'll need an evaluation board for access to the ADC. You should also use two low-pass filters or band-pass filters of the same make and model before the splitters, which will limit any wide-band noise from the signal generators.
Consistency in analog signal paths will minimize measurement errors. Cables must be the same type and length both before and after the splitter. You can easily see the cable length from the signal generator to the splitter need to be the same. Cable lengths after the splitter (going to both the ADC and the oscilloscope) can be misleading and require the same lengths too to preserve the measurement. If the evaluation board has any trace length from the connection point onto the board to the pins of the ADC, you must replicate that length from the splitter to the oscilloscope as well. Therefore, the cable lengths going from the splitter to the oscilloscope may need to be a slightly different length to accommodate any trace differences. Equal signal paths ensure that the signal you view on the oscilloscope will be an accurate representation of what is at the ADC’s analog input pins.

Although it seems the recommended method would be to solder your oscilloscope probe leads directly to the ADC’s analog inputs—which will give you the correct length matching—that may cause fluctuation in the measurement because doing so adds parasitic capacitance and inductance at the ADC’s probed analog input. Proper probing, combined with cables and splitters, will minimize the parasitic capacitance and inductance, producing a cleaner signal on the oscilloscope.

Make sure to use the proper bandwidth oscilloscope to display the differential analog input test frequencies. Remember to monitor each signal generator at all times without degrading the test signal. You can use an oscilloscope's math functions to ensure the proper phase and amplitude relationships between the two signals. That is, SignalA +
SignalB should be as close to 0 V as possible when the differential inputs are 180° out of phase. The sum of the signal amplitudes should, of course, increase as the signals drift from 180 degrees, but you should still use the signal across all phase offsets. That lets you establish the correct phase reference point (180° out of phase) from which to start the test.

The evaluation board needs a clean clock signal. Make sure to use a low-phase-noise oscillator or signal source so that you don't limit the ADC's performance. At Analog devices, we used, a 250-MHz Wenzel crystal oscillator in combination with a TTE 250 MHz band-pass filter. Figure 2 shows, from left to right, the oscillator, filter, and high-speed ADC evaluation board.

![Figure 2. Sampling Clock Setup consists of (l-r) an oscillator, low-pass filter, and ADC evaluation board.](image)

As the ADC's analog inputs drift out of phase on the oscilloscope, the power at the ADC's input signal fundamental frequency will decrease slightly, caused by the differential amplitude mismatch between the two signals. You should monitor the test frequency's fundamental frequency's level using an FFT (fast-Fourier transform) across all phase changes. Make slight amplitude adjustments to ensure that the ADC runs at the same level at all times. Differences in fundamental power can lead to inaccurate results, showing the ADC to perform poorly as phase and fundamental power become inaccurate.

Figure 3 shows two FFT readings using ADI's Visual Analog software (a free download at [www.analog.com/fifo](http://www.analog.com/fifo)) of the same part run at the same frequency. Figures 3a and 3b highlight the difference in amplitude of the fundamental frequency when the phase difference between the two input signals is 0° (Figure 3a) and when the difference is 20° (Figure 3b), where power in the second harmonic has increased.
Figure 3. a) Power in the second harmonic (marked “2”) increases when the phase difference between two input signals shifts by 20° (b).

Test Procedure

To begin the test, set one of the signal generators to produce a signal with the phase offset equal to 0°. Set the other signal generator so that the oscilloscope displays two waveforms 180° out of phase. With the amplitudes of the waveforms set close to one another and the frequencies exactly the same, use the oscilloscope math function (Channel A + Channel B), which will display a flat line, essentially 0 V. Notice the signal generators may not necessarily be set exactly the same amplitude based on the generator’s own tolerance. Any differences here are caused by the signal generator’s own reference gain and phase errors relative to frequency. Therefore, you must use an oscilloscope to null out phase or amplitude so you can minimize measurement errors. Next, you can sweep the signal generator with the 0° phase offset between +30° to –30° while holding the phase of the other signal generator constant.

You will need to choose some fundamental power and maintain it throughout the test. For this experiment, I set the fundamental signal’s power to –6 dBFS on each signal generator. With the fundamental signal’s power set, you should check the phase and amplitude of both signals with the math function on the oscilloscope. The peak-to-peak level of the math function should be as close to zero as possible. Once the measurement system is in balance, use this as your 0° out-of-phase reference start point.

The test should include saving the ADC’s second and third harmonic performance at every degree out-of-phase over a +30° to –30° range from the reference point where the signals are 180° out of phase. As the phase difference between the two signals drifts from 180°, the power of the carrier signal will drop as previously shown in Figure 3. Therefore, the output amplitudes of both signal generators are needed to keep the fundamental signal’s power level constant. Verify the signal amplitude using an oscilloscope to display the signals in the time domain after any adjustment. Once you collect 30 data points (1° offset through 30° offset), set the signal-generator output levels so that their signals are again 180° out of phase and readjust the amplitudes to ensure no unknown drift in amplitude or phase has occurred. Repeat the procedure for the –1° through –30° offset from the 0° reference point.
Perform the measurements over the useful bandwidths of the converter or its intended application. We used input frequencies at 2 MHz, 70 MHz, 170 MHz, and 300 MHz in this experiment. I adjusted the filter bandwidths before the splitter accommodate the appropriate bandwidth for the tested signal.

Test Results

Figure 4 shows a collection of normalized data from 2 MHz to 300 MHz input frequencies. The low frequencies have more tolerance to phase imbalance than higher frequencies. The graph shows that harmonic power increases with frequency. These measurements display a relative measurement and they don’t intend to show true performance of the ADC but for you to understand the trends that take place when analog input signals become phase imbalanced.

Figure 4. Second harmonics at low frequencies have less power than second harmonics at high frequencies.

Because the phase changes in both positive and negative directions provide similar results, the harmonics from the positive shift and the negative shift were averaged together and normalized to a zero point. The experiment lets you see the direct effect phase had on the device’s second harmonic performance as frequency is increased.

The topographic plot in Figure 5 compares phase deviation versus analog input frequency versus second-order harmonic performance. As phase deviation increases, a degradation of the input signal (in dB) will occur across all frequencies. That's shown by the increase in amplitude of the input signal's second harmonic.
Figure 5. The plot shows 2\textsuperscript{nd} Harmonic power versus frequency and phase deviation.

Figure 6 shows the normalized input signal's third-order harmonic performance for each frequency similar to that of Figure 4. The impact on the third-order harmonic versus phase deviation is much lower than for the second harmonic. At both low and high frequencies, the converter’s performance is flat relative to any phase deviation.
Figure 6. Power in the third harmonic shows little difference regardless of frequency.

Figure 7 is a topographic plot of the averaged third-order harmonic performance. Simply looking at the difference in the scale you can see the third-order harmonic converter performance is less dependent on frequency phase deviation as the second-order harmonics. That’s because of the ADC’s odd order nonlinearities are more inherent to the converter’s response to its trim, calibration, design, or process limitations.
Figure 7. Harmonic power versus frequency and phase offset shows that power increase as a result of phase, not frequency.

Conclusion

These measurements further verify that even-order distortion depends on balance and symmetry. These set measurements also show that in order to achieve datasheet performance the frontend input network design needs to be within ±3–4 degrees phase deviation from one analog input to another (typically referenced as AIN+/– or VIN+/–) at the ADC’s analog input pins.

The system design implementation that precedes the converter, be it a transformer, an anti-aliasing filter, or amplifier-driven circuit, that connects to the analog inputs affect ADC performance very much. As long at the input signals present at the outputs of these circuits are well balanced when connected to the converter, you can expect datasheet performance. You shouldn’t expect the second-order harmonic to be the limiting factor in the system’s dynamic range.

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**The effect of mismatched cables**

Keeping the setup consistent throughout the measurement process will greatly reduce the chance of inconsistent results. Signal generators, cable length, cable type, splitters, and filters all have to be evenly matched. This includes the slight additional trace length on the evaluation board to the converter. **Figures A and B** compare how mismatches can cause slight phase shifts and produce inaccurate measurements.

In addition to the details in the test set-up, you must also consistently monitor the measurements. For example, fundamental power fluctuations and slight phase/amplitude drifts from the signal generators can cause issues too. The oscilloscope lets you monitor these errors and you should be used at all times to monitor the analog input signals.

![Figure A. Mismatched cables can result in phase shifts that vary with signal frequency.](image)

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Figure B. Differences in signal-generator amplitude also produce frequency-dependent phase shifts.