**PRODUCT TRYOUT**

The incredible shrinking $199 DSO

I recently purchased a small digitizing oscilloscope, the “DSO Quad,” from Seeed Studio. While this instrument may seem to merit consideration as a toy or, at best, a conversation piece, some of the specs are certainly worthy of the $199 price. I’m impressed that the entire product, plus the rechargeable LiPo (lithium polymer) battery, fits into such a small package.

The unit, which is slightly larger than a standard business card, comes with two Mueller 10:1, 100-MHz probes with tiny MCX RF coax connectors. The DSO Quad has two analog channels and two digital channels. The sampling rate is 72 Msamples/s. I measured a bandwidth of about 3 MHz.

The vertical scale is adjustable from 20 mV/div to 10 V/div (8-bit resolution), and the horizontal sensitivity is 0.1 µs/div to 1 s/div. Input coupling is AC or DC, and triggering is Auto, Normal, and Single. There are several trigger modes: rising/falling edge, pulse width, and level.

The DSO Quad uses an ARM Cortex-M3 (32-bit) processor and integrated FPGA with a high-speed ADC. There’s an internal 2-Mbyte USB-connectable RAM for waveform storage and instrument setups. The 3-in. screen displays channel and setup information along the top and displays automatic measurements (V_{MIN}, V_{MAX}, V_{PP}, V_{DC}, V_{RMS}, and V_{BATT}) along the right side. The unit can also perform channel math functions such as A+B and A–B. The user can control all of these instrument configurations through toggle switches and a row of buttons along the unit’s top edge.

In addition to being a digitizing oscilloscope, the DSO Quad is also a signal source. It has two built-in signal generators, an 8-MHz variable-duty-cycle square-wave generator, and a 20-kHz function generator (sine, triangle, and sawtooth). These signals come out through a separate connector.

The DSO Quad is available through www.seeedstudio.com/depot (under “Hacking & Measurement”). The DSO Quad’s firmware is open source, and an active group of beta testers and other hobbyists develop additional functionality and make bug fixes. You can download periodic firmware updates from the user group page and load them through the unit’s mini-USB connector (bit.ly/KKHyt). A YouTube video demonstrates the basic operation (bit.ly/IJk500).

Ken Wyatt, Wyatt Technical Services

**OP-AMP TEST**

Understand key ADC specs

ADCs are the engines that drive digitized measurements. These devices are found in test and measurement products as well as equipment such as industrial and medical instrumentation. So, even if you don’t design measuring equipment but just use it, you should have an understanding of the specs that affect an ADC’s performance.

Noise, ENOB (effective number of bits), and effective resolution are three important ADC parameters. These parameters become more significant as measurement products and systems move from SAR (successive-approximation register) ADCs, which typically produce 12 bits and 16 bits, to sigma-delta ADCs, which produce up to 24 bits.

As the number of bits increases, noise plays an increasingly important role, because the voltage range of each bit shrinks. A given noise level that has essentially no effect on a 12-bit ADC has a significant effect on a 24-bit ADC. On top of that, ADCs run at ever-smaller voltage ranges, and they may need PGAs (programmable-gain amplifiers), which amplify noise as well as signals. Noise, therefore, reduces ENOB and effective resolution, which are defined as:

\[
\text{ENOB} = \log_2 \frac{\text{Full-scale voltage range}}{\text{ADC full-scale noise} \times \sqrt{12}}
\]

and

\[
\text{Effective resolution} = \log_2 \frac{V_{IN}}{V_{RMS \, \text{NOISE}}}
\]

Sigma-delta ADCs oversample a signal, then apply filtering and data decimation to achieve their final outputs. That technique, shown in the figure, lets the converter reduce noise. A designer can optimize the ADC by making tradeoffs between...
A sigma-delta ADC oversamples a signal, then applies digital filtering and data decimation to produce the final digitized representation of the analog input.

A low-noise oscillator is made from discrete components and op amps.

**AUDIO TEST**

**Build a circuit to test ADCs**

Today’s 20-bit to 24-bit ADCs need low-distortion signals for testing how well the ADCs digitize analog signals. Distortion in the source signal will add to any distortion that the ADC produces. Thus, low-noise signals are critical.

When he couldn’t find an oscillator with sufficiently low distortion, Vojtěch Janášek, an engineer at Janascard in the Czech Republic, built his own. The figure shows the oscillator, which produces distortion that’s more than –140 dB below the oscillator’s fundamental output signal. In addition, Janášek designed a notch filter that removes the oscillator’s fundamental frequency. That lets him view the distortion produced by the ADC.

The oscillator uses an inverted Wien-bridge topology with amplitude stabilization through an LED-driven CdS (cadmium–sulfide) photocell isolator. Using SPICE simulations before building the circuit, Janášek showed how the oscillator’s voltage noise-spectral density is highest at its resonant frequency, then falls at higher frequencies.

To verify the performance of his oscillator and filter, Janášek connected the final test signal to a data-acquisition system and frequency-analysis software. This particular module has a 14-bit ADC with a 400-ksamples/s sample rate. The module averages eight samples to reduce sampling speed to 50 ksamples/s and takes 128 ksamples to perform spectral analysis. Janášek’s measurement showed that the circuit’s THD (total harmonic distortion) is –145 dB.

The online version of this article (www.tmworld.com/2012_06) contains a link to Janášek’s article “Low-distortion oscillator tests measurement circuits,” which includes schematics for both the oscillator and filter circuits, plus plots of their performance.