ADC Guide, Part 3: Offset Errors

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Previous installments of this series discussed the sampling rate for an ADC. This time, we’ll explore offset error and ways to deal with it.

For an ideal ADC, the output code for 0V input will be all 0s. However, this will not be the case for a real-world ADC. Offset error is the constant error seen across the ADC’s range (Figure 1). (Note: we'll use a three-bit converter for simplicity, but the principles extend to higher resolution ADCs, of course).

Offset error can be positive or negative, and the ADC can be calibrated to compensate for it. However, there is a major disadvantage with calibration when the offset is very high. As seen in Figure 1, the output of the ADC corresponding to 0V input is 001 due to offset error. As a result, the output corresponding to input voltage 5.25V and above is 111.

Here, offset can be removed by deducting the zero-input code from the output of ADC. However, this reduces the ADC’s usable input range from 7.5 volts to 6.25 volts. For applications where the complete input range is required, this approach is not viable.
Calibrating single-ended ADCs

Accurately eliminating offset error from ADC output requires measuring the ADC offset and then adjusting for the offset error during normal operation. To measure the offset error for single-ended ADCs, the ADC input must be connected to an accurate and precise voltage source.

In case of a positive offset, the ADC output will read a non-zero value even when the input is connected to the GND. With a negative offset, the ADC will read 000 for non-zero input voltages, though it is above the minimum measurable input. For a positive offset, increase the voltage until the output code changes from 000 to 001.

In the case of a positive offset, a 0V reading will give the offset value. A negative offset can be calculated from the ideal ADC output at the voltage where the output of ADC makes its first transition. In Figure 2, the ADC output changes from 000 to 001 at 1.75 volts. At this voltage, an ideal ADC should have had an output count of 010. Therefore, this ADC has a negative offset equal to 010 minus 001, or 001, counts.

![Figure 2: Calibrating a single-ended ADC with negative offset](image)

For a single-ended ADC, run-time calibration can be difficult since there needs to be a voltage source which can be controlled. Also, the accuracy of the ADC will depend upon the accuracy of the voltage source. In general, single-ended ADCs are calibrated manually at the time of manufacturing, and their offset value can be stored in nonvolatile memory, such as Flash or EEPROM.
Calibrating differential ADCs

Calibrating the offset error for a differential ADC is an easier process since an external source is not needed to calibrate, even if the ADC has a positive offset or negative offset. This is because the ADC itself can give a signed output; just subtract the ADC value corresponding to 0V, when both inputs are shorted and connected to GND.

Offset drift

Since offset error varies with temperature, one-time offset calibration of the system will result in degraded accuracy. The offset error will need to be calculated more frequently and needs to be subtracted from the measured value of the signal.

This is especially important in the applications where the system is exposed to frequent temperature changes. For some applications, the offset error may need to be recalibrated before every valid measurement.

One effective technique for compensating for offset and offset drift is Correlated Double Sampling (CDS). CDS not only addresses offsets, but also compensates for low-frequency noise.

With CDS, the reference voltage is measured first by shorting both inputs. Next the input voltage is measured. When the direct input signal is measured, it will include the actual input voltage, noise voltage, and offset (Equation 1). Reference readings include the noise and offset (Equation 2):

\[ V_{\text{Input Signal}} = V_{\text{input}} + V_N + V_{\text{offset}} \]  \hspace{1cm} (1)
\[ V_{\text{Ref}} = V_N + V_{\text{offset}} \]  \hspace{1cm} (2)

A reference-input sample measured just before the current input measurement is given by Equation 3:

\[ V_{\text{Ref_prev}} = (V_N + V_{\text{offset}}) \times Z^{-1} \]  \hspace{1cm} (3)

The difference between the current input-voltage measurement and the previous reference signal is given by Equation 4:

\[ V_{\text{signal}} = (V_{\text{input}} + V_N + V_{\text{offset}}) - (V_N + V_{\text{offset}}) \times Z^{-1} \]  \hspace{1cm} (4)

\( V_{\text{offset}} \) is static, so its value for the current sample is the same as the value for the previous sample. But \( V_N \) is not static: this is the noise and drift term to be eliminated. Subtracting the previous noise term from the current sample will remove low-frequency noise and drift.

Though CDS proves to be a useful technique for compensating for offset and low frequency noise in an ADC/signal chain, it imposes limitations on the maximum effective sample rate for the actual signal, since two signals are being measured instead of one. This limitation becomes more dominant in ADCs like using delta-sigma topologies, where the modulator needs to be flushed whenever the channel is switched.
As a result, CSD is mainly used in very-low-frequency applications such as temperature measurement and strain-gage applications. In these cases, the required sample rate is generally very low and implementing CDS does not create any issues.

Also, CDS can be implemented effectively in devices where multichannel ADCs are an integrated part of the controller. For example, PSoC devices from Cypress have built-in ADCs and the input channel can be switched quickly. Also, the availability of an internal reference enables the use of only a single pin for single-ended applications, and just two pins for differential modes, thus avoiding the need for an extra pin for a reference measurement.

The next part of this series will discuss gain error.

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