ADC Guide, Part 6: Common mode input, CMRR, and PSRR

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This part of the article series talks about the common mode input voltage range, common mode rejection ratio and power supply rejection ratio of an ADC.

Common-mode input range: The common-mode signal is the input voltage that is connected to both the positive and negative input terminals of an ADC. It can be considered as in-phase and that the same amplitude signal is connected to both terminals. The common-mode input range for an ADC, generally referred to as $V_{CM}$, is defined as the maximum common mode voltage that can be applied to both inputs of a differential ADC for a valid measurement.

In many systems – for instance, AM/FM receivers – common-mode voltage is nothing but the DC offset provided from the differential output stage in a single-supply system. DC offset is applied because the signal cannot go negative with respect to system ground. The common-mode input range specification limits the maximum DC offset for these signals.

Based on the application, designers either need to select an ADC which supports the required common-mode voltage or design an interfacing circuit to deal with the limited common-mode input range of the ADC. Today, many ADCs are available that support a common mode voltage close to the power supply rail to help in avoiding design complications.

Common-mode input voltage comes into the picture when the signal is referenced to the ground that is the same as that of ADC. If the signal source’s ground is isolated from the ADC’s ground, then DC offset will not cause an issue because, in this case, the only differential voltage comes across the ADC’s input. Thus, the simplest way to deal with the common-mode signal is to isolate the signal source from the ADC using a transformer, or to have independent power supplies/batteries that do not have grounds connected.

Common-mode rejection ratio: Common-mode rejection ratio (CMRR) is one of the most commonly used specifications for analog circuits. For ADCs, this specification is given when the ADC is being used for differential measurement. CMRR for an ADC is the capability to reject common-mode input voltage.

As discussed earlier, in many applications the input is AC and will have some component which is negative with respect to ground. However, an input which is below the ground rail cannot be applied to most ADCs for safe operation. Thus, a DC offset needs to be provided to the input signal and that offset becomes the –ve input for the ADC.

For an accurate measurement, the ADC must be capable of completely rejecting that DC offset (common mode signal). A high value of CMRR is preferred. CMRR is defined as the ratio of the differential gain versus the common-mode gain:

$$\text{CMRR} = \frac{A_{\text{Diff}}}{A_{CM}}$$  \hspace{1cm} (Equation 1)
where $A_{\text{diff}}$ is the differential gain and $A_{\text{CM}}$ is the common-mode gain.

In context with ADCs, the differential gain is defined as:

$$A_{\text{Diff}} = \frac{\Delta \text{Output Code}}{\Delta \text{Differential Voltage}} \quad \text{(Equation 2)}$$

and the common mode gain is defined as:

$$A_{\text{CM}} = \frac{\Delta \text{Output Code}}{\Delta \text{Common Mode Voltage}}. \quad \text{(Equation 3)}$$

In ADCs, since the output code change is very small with respect to the common-mode voltage, the CMRR is generally a large number and therefore is expressed on a logarithmic scale. So, for ADCs, CMRR is given by **Equation 4**:

$$\text{CMRR}_{\text{ADC}} = 20 \log \left( \frac{A_{\text{Diff}}}{A_{\text{CM}}} \right). \quad \text{(Equation 4)}$$

At low frequency (or, we can say at nearly the DC input signal), a low CMRR can be dealt with correlated double sampling as was discussed in previous parts of this series. The only care that must be taken is the reference voltage to be used for taking a zero input sample. This voltage has to be the common-mode voltage used at the time of the measurement.

However, it is hard to deal with bad CMRR when the frequency of the common-mode signal increases. CMRR is a function of the common mode signal’s frequency. As the frequency increases, CMRR becomes worse. CMRR is generally specified at 60Hz, which is the line frequency.

**Power-supply rejection ratio:** Generally for ADCs, the power-supply rejection ratio (PSRR) is one of the overlooked specifications. However, it is an important specification that defines the system’s overall noise performance and accuracy. PSRR for any analog circuit is the measure of its immunity to power-supply changes. A high PSRR is needed for higher rejection to power-supply changes.

PSRR for an ADC is measured as the ratio of the change in the power-supply voltage to the change in the output voltage that is voltage equivalent to the output counts. So, PSRR for an ADC is given as **Equation 5**:

$$\text{PSRR} = 20 \log \left( \frac{\text{change in supply}}{\text{change in output voltage}} \right) \quad \text{(Equation 5)}$$

For example, if the power supply is changed from 4V to 5V and this results in a 1mV change in output, then PSRR will be given by:

$$\text{PSRR} = 20 \log (1/0.001) = 60 \text{ db} \quad \text{(Equation 6)}$$

As of now, PSRR discussed is the DC PSRR, and it is only useful in applications where the change in power supply is slow due to degradation in battery voltage, voltage drift in the voltage regulator with time, or temperature, and there is no noise on the supply. Though this value of PSRR is useful in fewer applications, this is the PSRR that is described in most of the ADC datasheets.
When there are ripples in the power supply due to the line frequency, external noise, or switching in digital circuitry, this makes PSRR worse. Due to stray capacitance, the AC component on the power rail gets coupled to the output, causing PSRR to degrade. To define AC PSRR, a signal of known amplitude and frequency is coupled onto the power rail. An FFT spectrum of the output is used to define the PSRR. This is the more useful specification when the power rail is noisy.

In the case of precision measurements, one may need to design the power supply appropriately to make sure that power-supply ripples do not affect beyond the system requirements. To remove noise from the supply and switching, decoupling/bypass capacitors must be placed close to the supply pins. Most applications that use 16-bit or higher resolution (for example, strain gauges) need a clean power supply to deal with PSRR and to achieve the required effective number of bits (ENoB) and, hence, need low-noise regulators.

Designing a low-noise power-supply increases the overall system cost. Based on the PSRR specified in the ADC’s datasheet and required system accuracy, one can decide on the power-supply requirements. Digital switching is one of the major causes of noise on the power lines and causes system’s performance to degrade. To deal with switching noise, analog and digital power supplies must be kept separate.

Future parts of this series will talk more about the noise and details on power supplies to achieve the best from the ADCs.

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