Tools for Embedded Developers

**Software**

**IDE for DSP**
Virtuoso v. 4.2 is an integrated development environment for the design of multi-processor embedded DSP networks, such as radar, sonar, and high-end image processing. It includes the Virtuoso RTOS, a project manager, a multi-threaded asynchronous host server, and a suite of graphical analysis and debugging tools, as well as plug-ins to Code Composer Studio and Visual DSP. The Virtuoso RTOS features a single processor programming style for multi-processor systems, communicating sequential processes (CSP), multithreading, multitasking capabilities, static memory allocation, target channels that allow data to be sent and received at different rates without buffers, and distributed, shared, or pooled memory architectures. In the CSP model, tasks communicate directly through channels that serve data-flow pipes. The channels exploit the multiple external buses or the direct link ports available on DSPs, so that the DSPs communicate directly with each other without using the system bus. Virtuoso v. 4.2 is available now. It costs $10,000 for single processor targets and $20,000 for virtual single processor support for multi-processor systems.

**Eonic Systems**
Brea, CA
(714) 255-8689
[www.eonic.com](http://www.eonic.com)

**RTOS for 8-bit PICmicro**
Real-Time Architect is an RTOS and development environment for the PICmicro family of 8-bit microcontrollers. It offers a preemptive kernel (SSX5) and associated development tools to provide the PICmicro developer with multitasking capabilities. The SSX5 run-time kernel has a memory footprint of as little as 1.6KB ROM and 300 bytes RAM in typical applications. Its capabilities include preemptive scheduling and real-time analysis and optimization, in addition to a range of optional application-specific development tools such as OSEK support for embedded automotive design projects. Real-Time Architect also provides a suite of timing analysis and optimization tools based around Time Compiler. Time Compiler establishes relationships between the worst-case response times of tasks and interrupt service routines, and their deadlines. It determines whether or not a system is schedulable and indicates the margin by which a deadline is met or missed. Real-Time Architect is available now.

**Realogy**
York, England
(44) 1 190-443-5129
[www.realogy.com](http://www.realogy.com)

**GUI library**
RTPEG-32 is an event-driven, object-oriented C++ GUI library for RTOS-32 embedded systems. It includes a set of controls that look and behave like those for Windows 95. Predefined classes include buttons, bit-maps, check boxes, scroll bars, menus, progress bars, and so on. In RTPEG-32’s event-driven programming model, an application’s user interface objects are typically C++ classes derived from predefined RTPEG-32 classes. Such derived classes can override methods such as Draw() to implement a custom appearance, or Message() to catch messages sent by a user input device, separate threads, or other GUI controls. A driver for VGA 16-color mode is included, as well as drivers for 8-bit, 16-bit, 24-bit, and 32-bit color depth with arbitrary resolution. RTPEG-32 supports mice, including any Microsoft Mouse-compatible devices, such as most touch screens. However, RTPEG-32 applications can also be navigated using only the keyboard. RTPEG-32 comes with the utility WindowBuilder, a prototyping and design tool used to create graphical objects such as bitmaps, fonts, windows, and so on. It generates C++ source code to initialize all designed windows and catch defined messages. Additional tools are included to generate custom fonts and to convert BMP, GIF, and JPEG images into compilable C++ source code. A developer’s license is $2,500. There are no run-time royalties.

**On Time Software**
Setauket, NY
(888) 667-8200
[www.on-time.com](http://www.on-time.com)

**MMU RTOS**
Integrity v. 3.0 is a scaleable, ROM-able real-time operating system that uses the hardware memory protection facilities of MMUs to separate the kernel and user tasks into separate address spaces. This effectively builds a firewall between the kernel and each user task, helping to prevent errant or malicious tasks from corrupting user data, the kernel, interprocess communications, device drivers, or other user tasks. The Integrity v. 3.0 kernel provides a number of features not available in previous versions, including a highest lock-er semaphore and ARINC 653 parti-
tion scheduling. Integrity also features multiprocessor debugging support, a simulation environment, an integrate utility, and support for a variety of Internet and telecom protocols, including TCP/IP, PPP, FTP, DHCP, ATM, SS7, Frame Relay, ISDN, H.323, V.5, and X.25. Integrity also supports Interniche’s Web server, browser, and TCP/IP stack, which makes it possible to embed Internet connectivity into target systems running the Integrity RTOS. Full source code for Integrity is available for $50,000, partial source code (for BSP) is available for $10,000.

Green Hills Software
Santa Barbara, CA
(805) 965-6044
www.ghs.com

pSOS API
The OnCore pSOS allows pSOS applications to run on top of the OnCore Microkernel within a memory management unit-protected partition. System designers can mix an array of enterprise and real-time applications without sacrificing mission-critical, real-time characteristics. Also provided is the OnVoy messaging system, which provides messaging between separate processors. OnVoy is an open specification that allows the layering of the OnCore distributed interprocess communication (DIPC) model on top of legacy environments. The pSOS API and OnVoy are royalty-free components that ship in both binary and source forms. They are available now.

OnCore Systems
Half Moon Bay, CA
(650) 712-0655
www.oncoresystems.com

Tool suite
The SLE88 Tool Suite v. 1.1 targets Infineon Technologies’ 32-bit Smart Card solution. Designed to optimize the SLE88’s security and performance capabilities, the tool suite enables designers to create operating systems that serve as a base for independent product development by third parties, as well as support for the execution of multiple applications. The SLE88 Tool Suite features a shared library concept that uses a development environment in which designers can tailor debugging capabilities to the application they are developing. It includes a C/C++ compiler, an assembler for the SLE88’s core and peripheral control processor, a linker/locator, and a post locator that builds applications by linking secure shared libraries in virtual memory space. The SLE88 Tool Suite v. 1.1 is available now.

Tasking
Dedham, MA
(781) 320-9400
www.tasking.com

ColdFire compiler
The CAD-UL C compiler now supports the ColdFire 5206e processor, allowing engineers to develop applications using CAD-UL’s ANSI C compiler products and tool suite. This tool suite features a C compiler that generates ROM-capable code, and supports applications that utilize both 16- and 32-bit integer size. The Tool Suite also includes an assembler and library and provides linker support within the Workbench integrated development environment. The compiler and tool suite for the MCF5206e are available now for Solaris 2.x and HP-UX host systems. They start at $2,200 per seat.

CAD-UL
Scottsdale, AZ
(877) 462-2385
www.cadul.com

Distributed OS
Plan 9 is an operating system designed for distributed computing in a networked environment. It uses a single protocol to refer to and communicate with processes, programs, and data, making it suitable for building large, distributed systems containing a number of file servers, CPU servers, and other components. It is designed around the basic principle that all resources appear as files in a hierarchical file system. These resources are accessed by means of a network-level protocol called 9P, which hides the exact location of services from the user. All servers provide their services as an exported hierarchy of files. Plan 9 has remote booting capabilities, which makes it possible to use PCs as user terminals. Additional features include the dump file system, which makes a daily snapshot of the filestore available to users; unicode character set support throughout the system; advanced kernel synchronization facilities for parallel processing; an ANSI/POSIX environment emulator; Acme, an editor, shell, and window system for programmers; Sam, a screen editor with structural regular expressions; and support for MIME mail messages and IMAP4. Plan 9 is available now and can be ordered from the company’s Web site. A CD version costs $25, the manual set costs $75, and the boxed set costs $100.

Vita Nuova
Montclair, NJ
(866) 835-8482
www.vitanuova.com

Development environment
The VisualDSP++ DSP development environment features a C++ compiler, an enhanced user interface, plotting tools that visually measure software performance, and statistical profiling to identify programming bottlenecks. VisualDSP’s debugger features data visualization implemented by a plotting package. This
enables the programmer to examine the performance of an algorithm. Statistical profiling lets the programmer non-intrusively poll the processor as it is running the program. The VisualDSP++ environment costs $2,995. It’s available now.

Analog Devices
Norwood, MA
(800) 262-5643
www.analog.com/dsp

**Hardware**

**Device Programmer**
The BP-1400 universal device programmer supports 15,510 device technologies. This includes SOIC, TSOP, TSSOP, QFP, TQFP, PQFP, SSOP, PGA, SIMM, PCMCIA, LGA, CSP, VSOP, PLCC, µBGA, FBGA, BGA, and DIP. It comes with 240-pin drivers standard and uses high-speed bipolar analog pin drivers with microstrip transmission lines to deliver 800ps rise times at the programming socket without, the company claims, overshoot or ground bounce. It’s available now for $8,995.

**BP Microsystems**
Houston, TX
(713) 668-2620
www.bpmicro.com

**Chips**

**DSP core**
The Super10 DSP microcontroller features an architecture that executes most instructions in one cycle. It’s code compatible with standard members of the ST10 series of cores, allowing already-designed software to be used in newer applications. The Super10’s target applications include control applications in hard disk drives, as well as automotive and consumer applications that require DSP algorithms. It features an interrupt jump cache, which allows the interrupt controller to transfer a 24-bit start address directly to the CPU for the service routine, without time overhead. The Super10 core can be operated at any speed up to 150MHz and features power consumption of 0.2mW/MHz to 0.5mW/MHz.

**STMicroelectronics**
Lexington, MA
(781) 861-2650
www.st.com

**USB chip**
The M3753x is a one-time-programmable, USB-compliant, 8-bit micro-

**New Products**
controller designed for cost-sensitive, low-speed (1.5Mbps) human interface computer peripheral applications. When the USB peripheral is not being used, the chip goes into a “USB suspend mode,” in which maximum power consumption is 300µA. Its typical operating current is 6µA, which equates to 30mW of power dissipation at 5V. It includes an external interrupt feature that enables designers to set the “key on wakeup” interrupt and counter terminals to even count mode; a minimum instruction execution time of 0.34µs; an analog-to-digital converter; up to 33 programmable I/O ports; serial I/O timers; and a watchdog timer. It’s available now.

Mitsubishi
Sunnyvale, CA
(408) 730-5900
www.mitsubishichips.com

**PC-compatibles**
The Atlas, the Consumer-II, and the Elite are members of the STPC family of PC-compatible system-on-chip devices. Based on the x86 architecture, the central component of these three devices is a 64-bit, 133MHz processor block, which contains a 64-bit SDRAM controller, a bus mastering EIDE controller, and a PCI local bus controller. The Consumer-II and the Atlas feature a VGA-/SVGA-compatible graphics accelerator, video input, and video port. The Consumer-II also features a PAL/NTSC encoder and a flicker filter. The Atlas includes a digital TFT LCD panel interface, making it suitable for use in Web-enabled appliances, such as Web-pads, Web-phones, POSes, and thin-client terminals. All three devices come in plastic BGA packages. The Atlas costs $38, the Consumer-II costs $33, and the Elite costs $26. The Consumer-II and the Elite are available now. The Atlas will be available in the first quarter of 2001.

STMicroelectronics
Lexington, MA
(781) 861-2650
www.st.com

**ADC/flash microcontroller**
The PIC167X family is a series of flash microcontrollers with integrated analog-to-digital circuitry. The PIC16F73 and the PIC16F74 offer 4Kwords of flash program memory and 192 bytes of data RAM. The PIC16F76 and the PIC16F77 offer 8Kwords of flash program memory and 368 bytes of data RAM. All chips in the series feature an integrated multi-channel A/D converter. Another on-chip peripheral is the timer subsystem, which provides a real-time clock or two 8-bit and one 16-bit counter/timer modules. The devices typically draw 20µA from a 5V supply while operating at 32kHz. A sleep mode instruction combined with the ability to switch off the A/D circuitry when it is not being used typically decreases current draw to less than 1µA. The communications features of the family include 22 or 33 pins for I/O functions; a synchronous serial port supporting SPU or PC protocols; 50Mbps universal synchronous/asynchronous receiver-transmitter with baud rate generator for serial communications; two pulse width modulator outputs with 10-bit resolution; and two 16-bit capture/compare modules. The PIC16F73 costs $3.43, the PIC16F74 costs $4.15, the PIC16F76 costs $4.86, and the PIC16F77 costs $5.22. They’re sampling now and will be available in production quantities in the first quarter of 2001.

Microchip Technology
Chandler, AZ
(480) 786-7200
www.microchip.com

**SoC**
The ARM966E-S is a system-on-a-chip device that runs at 200MHz using an ARM processor. It’s designed for use in communication systems that need deterministic control and digital signal processing capabilities. These might include mass storage, next-generation digital cellular phones, or networking applications. The ARM966E-S uses the Thumb instruction set. It is available now on G12 0.18-micron drawn technology.

L5I Logic
Milpitas, CA
(800) 433-8778
www.lsil.com

**RISC DSP**
The E1-32XS RISC DSP uses a single-processor and single data stream model. It’s a 32-bit microcontroller that features static design and runs at 180MHz. The E1-32XS is designed for use in portable multimedia and consumer electronics products, such as wireless PDAs, digital cameras, MP3 players, and handheld GPS devices. It features an on-chip DRAM controller that interfaces to external memory; an on-chip hardware timer coupled to a clock by means of a programmable pre-divider; and an operating temperature range of 0 to 70 degrees Celsius for commercial use and -40 to 85 degrees Celsius for industrial use. The E1-32XS is available now.

Hyperstone Electronics
Commerce, CA
(323) 726-8833
www.hyperstone-ag.com

**Radiation-tolerant chip**
The TSC695E is a single-chip version of the ERC32 32-bit radiation-tolerant processor. The standard version of the TSC695E delivers up to 20 MIPS. It has single event upset immunity and total dose tolerance in excess of 300 Krad. Running with supply voltage between 3V and 5.5V, the TSC695E is available in 256-pin quad flat pack or die form.
IAP chips
The KX8 and KX2 are members of the 68HC08 family of 8-bit microcontrollers. They are in-circuit and in-application programmable. They feature an internal clock generator that can be programmed in the application to a specific target frequency. These two chips offer analog capability in the form of a four-channel, 8-bit analog-to-digital converter. Additional features include 192 bytes of RAM; and a two-channel, 16-bit timer interface module (TIM). The flash memory on the KX8 and KX2 is capable of write/erase cycling to 10,000 cycles and programming at up to 2ms for a 64-byte block. The KX8 costs $2.70. The KX2 costs $1.95. The KX8 and KX2 chips are available now.

Motorola
Austin, TX
(512) 895-9705
www.motorola.com/sps

Single-board computer
The Bitsy is a single-board computer with a 3-by-4 in. footprint. Targeted for the PDA/Handheld markets, the Bitsy is built around the 32-bit StrongARM SA-1110 RISC processor and SA-1111 companion chip. The processor runs at less than 450mW at 206MHz. The system runs unregulated from 6 to 12VDC, includes a battery charger, and supports a backup battery. The Bitsy also supports up to 16MB of SDRAM and 32Mbits of flash memory and includes a Type II PCMCIA slot. Its I/O and communication options include three serial ports (configurable as RS-232, TTL, and IrDA), USB master and slave, audio input and amplified stereo output, and touchscreen support. The Bitsy includes 12 digital I/Os, four analog inputs, and nine additional digital I/Os that can be configured as a 4-by-5 keypad. Bitsy's graphics features include backlight control, Vee generation, and interfaces to flat panels up to 1024 x 1024 pixels and 16-bit color. It will be available in the first quarter of 2001. Bitsy costs $300 per unit.

Applied Data Systems
Richardson, TX
(972) 238-8111
www.applieddata.com