Recover the leakage energy of a flyback transformer

Todor Arsenov, Spellman High Voltage Electronics Corp, Hauppauge, NY

The classical technique for demagnetizing the transformer in any forward converter is to implement a second winding bifilar with the primary winding to ensure continuous flow of the magnetizing current when the power switch (typically a power FET) turns off. Such a circuit generally limits or clamps the FET’s drain-to-source voltage to two times the dc supply-rail voltage. The same technique—using this recuperating winding—can be successfully implemented in a flyback topology to deal with the leakage-inductance problem.

Note that in any flyback converter, the flyback transformer (multiwinding inductor) is far from perfect; leakage inductance (primary to secondary) is as much as 5% of the magnetizing primary inductance\(^1\). The leakage inductance \(L_{LK}\) is effectively in series with the power FET (drain connection). Complicating matters, the parasitic output capacitance of the FET \(C_{oss}\) forms a series-resonant circuit with \(L_{LK}\). When the FET turns off, very high overvoltage and ringing can occur. The higher the Q of the circuit, the higher the ringing voltage. This situation will likely cause significant EM interference and, due to the elevated FET drain voltage, lower the FET reliability.

Figure 1a shows a flyback converter with such a recuperating winding added on a modified demonstration board (STMicroelectronics’ Viper17L\(^2\)). Some important considerations: Resistors \(R_{S1}\) and \(R_{S2}\) are sense resistors used for monitoring the currents; scope measurements for currents are measured directly across these resistors. The transformer ratios are the same as in the original transformer. The recuperating winding, \(N_R\),

![Diagram of flyback converter with recuperating winding](image-url)
is magnetically coupled tightly to only the primary winding, \( N_p \), by making these two windings bifilar. Bifilar windings are made by simultaneously winding two wires side by side around the magnetic core, or bobbin; this approach maximizes coupling and tightly matches the parasitic capacitance and inductance. The coupling between the primary and the other windings is not as important.

In Figure 1b, it can be seen that without any clamping (\( D_3 \) disconnected), the voltage at the FET’s drain (IC1, pins 7 and 8) due to the ringing reaches 560V peak. The primary current is shown magnified in Figure 2a. At the moment the FET turns off, the primary current (magnetizing current) remains constant, charging the capacitance, \( C_{\text{Oss}} \). This is indicated by the step waveform. The magnetizing current remains constant, as diode \( D_4 \) on the secondary side is still not conducting; this can be seen from the secondary current waveform in Figure 2b. The short period of time after the turn-off (when \( D_4 \) is not yet conducting) is the time when the series-resonance circuit’s \( C_{\text{Oss}} \) is charged. Corresponding to the time when the FET’s drain voltage, \( V_{\text{DS}} \), becomes high

Figure 1b Without any snubbers, the ringing on voltage (Channel 1, blue) and current (Channel 2, red) waveforms can be quite big.

Figure 2 In these results from the series tank circuit, there is ringing at the FET’s drain (\( V_{\text{DS}} \), Channel 1, blue) after the primary current (Channel 2, red) charges \( C_{\text{Oss}} \) following turn-off (a). \( V_{\text{DS}} \) is again shown as Channel 1; the charging of \( C_{\text{Oss}} \) delays the secondary current through \( D_4 \) (Channel 2) by just under 100 nsec (b). The bifilar winding, \( N_p \), steers the primary current (Channel 2) back to the power rail and clamps the switch voltage (Channel 1) (c). The leakage flux fights the current transfer; the secondary current (Channel 2) rises to an equilibrium peak value until the leakage energy is fully recuperated (d).
Double the protection of a laser driver using a 1V power supply

Tai-Shan Liao, National Applied Research Laboratories, Instrument Technology Research Center, Hsinchu, Taiwan

An excessive level of light from a laser pointer, even if only for a short duration, can be harmful if it enters the human eye either directly or through reflection from a shiny object. Most countries, therefore, have laser safety requirements that limit the maximum emission level. This Design Idea describes a laser driver that works even with a single 1.5V cell discharged to 1V, and uses dual current-control transistors to improve reliability against shorting and allowing excessive laser current and light emission.

In Figure 1, the transistors Q1, Q2, and Q3 compose a negative impedance, which can be described approximately as \( Z = -\beta(\Delta V_{BE}/R_F) \). Assume that all of the transistors have the same current gain \( \beta \), and \( V_{BE} \) is the base-to-emitter voltage of all transistors. Feedback is provided through \( R_F \), and \( R_L \) bias controls the collector current of Q4. Inductor \( L_1 \), and parasitic capacitance form a resonant circuit that oscillates due to the negative impedance, resulting in about 3.5V pk-pk at Q4’s collector, with the battery at 1V. Schottky diode \( D_1 \) and \( C_1 \) form a half-wave rectifier that provides about –3V for the laser cathode; with \( V_{DD} \) at 1V, this provides a 4V working range to overcome the laser threshold.

Q1 and Q2 control the laser current. The photodiode built into the laser assembly monitors the light intensity and sends negative feedback through \( Q_5 \) to bias \( Q_5 \) and \( Q_6 \) to the proper collector current for the constant desired laser intensity. The \( Q_5 \) and \( Q_6 \) pair is series connected so that if one should fail shorted, the other will still maintain the laser current at a safe level. The probability of failure of two transistors at the same time is far lower than the probability of failure of a single transistor.

Editor’s note: Due to variations in laser and photodiode efficiency, \( R_7 \) might need to be adjusted to ensure the laser output is within safety-regulation limits.

REFERENCES

Figure 1 You can use this dc-dc step-up circuit and dual current-control transistors to safely power this laser from an almost-discharged battery.
Oftentimes the biggest obstacle in designing an isolated dc/dc converter is the transformer design, a prospect that sometimes discourages designers from undertaking an otherwise straightforward design task. You can take advantage of the characteristics of an off-the-shelf gate-drive transformer and produce four separate isolated dc outputs. Gate-drive transformers are actually ideal for low-power dc/dc power transfer, because they have already been optimized for a high product of voltage and time (ET, or volt-microsecond, product) as well as for low leakage inductance.

A core with high permeability and low core loss at high switching frequency (F_{SWX}) supports the typical 10 to 15V applied primary voltage and the typical 500-nsec to 5-μsec on-time of switching frequencies between 100 and 500 kHz. This range of voltage and time is in the range needed for this dc/dc design. Also, a core geometry and winding configuration has already been chosen for low leakage inductance in order to produce fast rise and fall times, as well as low ringing. Lastly, the wire gauges used are sufficient for dc/dc-converter applications handling winding currents in the tens-of-milliamps range without excessive copper losses.

The Pulse Electronics P0585 gate-drive transformer has five windings, each with an identical number of turns. One winding is wound with triple-insulated wire (TIW); the other four windings are standard magnet wire. You drive the TIW winding as the primary to provide a 3-kV RMS primary-to-secondary breakdown rating. The breakdown voltage rating between the four secondary windings is not specified, but this type of wire insulation is typically used in offline supplies where up to 400V can be seen between windings.

Isolated outputs offer great flexibility. They provide a convenient way to break ground loops, power remote circuits at different ground potentials, and allow for simple negative or positive output voltage polarity selection. Figure 1 shows the four secondaries of this transformer, creating four separate, equal-voltage outputs. You can, however, wire these secondaries in various series/parallel combinations to produce a myriad of output voltage/current combinations.

The Maxim MAX13256 H-bridge transformer driver (IC 1) is an ideal part for this application. It incorporates all of the functions needed for a standalone, transformer-isolated dc/dc converter. Its internal FETs withstand 36V and are configured as two separate push-pull outputs, which drive a transformer primary with a precise 50% duty cycle to avoid core saturation. It also incorporates adjustable and robust internal current limiting, so the outputs are protected against short circuits and recover nicely.

Figure 1 IC 1 drives the transformer primary with a 50%-duty-cycle square wave to avoid core saturation.
upon fault removal. It also incorporates undervoltage lockout (UVLO) to prevent switching activity when the input voltage is too low.

The Linear Technology LTC6900 clock source (IC₁) was added to allow precision adjustability of the switching frequency. The MAX13256 does have an internal clock, but most users would probably prefer to set the switching frequency themselves for overall system compatibility or EMI reasons. The MAX13256 accepts an external TTL-level clock, and its UVLO feature ensures that IC₂ is up and running before the ramping VIN of its UVLO feature sets itself for overall system compatibility or EMI reasons. The MAX13256 does have an acceptability or EMI reasons. The MAX13256 drives the transformer primary with a precise 50% duty cycle, that voltage is present (on-time). Since the MAX13256 drives the transformer primary with a precise 50% duty cycle, the maximum ET product will occur with a 15V input voltage. At the lowest switching frequency of 100 kHz in this case, the maximum on-time at 100 kHz is 5 μsec. The maximum ET product is therefore 75 μVsec, which meets the specification.

Following is a brief tutorial on checking the transformer operating parameters against the data-sheet specifications. The P0585 transformer has a maximum ET product of 95 μVsec. This calculation is the product of the maximum voltage impressed across the primary winding and the maximum time that voltage is present (on-time). Since the MAX13256 drives the transformer primary with a precise 50% duty cycle, the maximum ET product will occur with a 15V input voltage. At the lowest switching frequency of 100 kHz in this case, the maximum on-time at 100 kHz is 5 μsec. The maximum ET product is therefore 75 μVsec, which meets the specification.

The peak flux-density spec is 2100 Gauss. To calculate peak flux density, equations 2A and 2B provided on the data sheet are based on V_IN and the equations 2A, "DON" is the duty cycle of 50%, or 0.5, not time in microseconds. Under these conditions, the calculated peak flux density is 1512 Gauss, which meets the data-sheet specification.

Core loss is calculated using the formula provided on the transformer data sheet. The results are 0.468W at 100 kHz and 0.117W at 500 kHz, which is lower than at 100 kHz due to the lower ET product.

The copper loss of 93.75 mW was calculated using the formula provided on the transformer data sheet. This simplified formula calculates copper loss based on IR losses in the windings and does not consider skin or proximity effects in the windings. Therefore, there is no frequency dependence in these simplified results, which are based on ±500-mA peak current in the primary winding and ±125-mA peak currents in each of the four secondary windings.

Using the temperature-rise formula from the transformer data sheet and the total losses calculated above (561.75 mW at 100 kHz), the predicted temperature rise of the transformer is 37.2°C.

This Design Idea uses the P0585 gate-drive transformer, but other (smaller) off-the-shelf gate-drive transformers can be used, especially if fewer outputs are needed, and at less current. Just be sure to check the transformer's maximum volt-μsec specification as in the example described here.

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**Table 1** Measured Results at Input Voltages of 10, 12, and 15V DC

<table>
<thead>
<tr>
<th>Switching frequency</th>
<th>Measurements</th>
<th>V_IN=10V DC</th>
<th>V_IN=12V DC</th>
<th>V_IN=15V DC</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 kHz</td>
<td>V_OUT at I_OUT (light load)</td>
<td>9.82V at 1.31 mA</td>
<td>11.82V at 1.58 mA</td>
<td>14.77V at 1.97 mA</td>
</tr>
<tr>
<td></td>
<td>V_OUT at I_OUT (full load)</td>
<td>8.19V at 110.29 mA</td>
<td>10.26V at 103.97 mA</td>
<td>13.17V at 111.51 mA</td>
</tr>
<tr>
<td></td>
<td>P_OUT at full load (each output, total)</td>
<td>0.9W, 3.61W</td>
<td>1.07W, 4.27W</td>
<td>1.47W, 5.87W</td>
</tr>
<tr>
<td></td>
<td>I_IN, P_OUT at full load</td>
<td>450.4 mA, 4.5W</td>
<td>428.28 mA, 5.14W</td>
<td>463.33 mA, 6.95W</td>
</tr>
<tr>
<td></td>
<td>Efficiency (P_OUT/P_IN) at full load</td>
<td>80.22%</td>
<td>83.07%</td>
<td>84.46%</td>
</tr>
<tr>
<td>500 kHz</td>
<td>V_OUT at I_OUT (light load)</td>
<td>12.92V at 1.72 mA</td>
<td>15.3V at 2.04 mA</td>
<td>18.74V at 2.5 mA</td>
</tr>
<tr>
<td></td>
<td>V_OUT at I_OUT (full load)</td>
<td>8.09V at 108.94 mA</td>
<td>10.2V at 103.36 mA</td>
<td>13.12V at 111.08 mA</td>
</tr>
<tr>
<td></td>
<td>P_OUT at full load (each output, total)</td>
<td>881 mW, 3.53W</td>
<td>1.05W, 4.2W</td>
<td>1.46W, 5.84W</td>
</tr>
<tr>
<td></td>
<td>I_IN, P_OUT at full load</td>
<td>445.45 mA, 4.45W</td>
<td>426.26 mA, 5.12W</td>
<td>461.72 mA, 6.93W</td>
</tr>
<tr>
<td></td>
<td>Efficiency (P_OUT/P_IN) at full load</td>
<td>79.33%</td>
<td>82.42%</td>
<td>84.13%</td>
</tr>
</tbody>
</table>

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**REFERENCE**

Two ICs form F/V converter

Peter Winship, University of California, Berkeley

Using only six components, you can configure a circuit (Figure 1) whose output voltage is proportional to its input frequency. Moreover, only three of the components—capacitor $C_0$, resistor $R$, and the OP-07 op amp—must exhibit low drift for stable operation over temperature. The circuit provides linear operation well into the megahertz region.

The average current ($I_{AVG}$) from the 40106 Schmitt-trigger inverter’s ground pin (pin 8) is linearly dependent on the frequency at which $C_0$ is discharged into the op amp’s summing junction. The op amp forces this current to flow through the 13.33-kΩ feedback resistor, producing a corresponding voltage drop. The output voltage is

$$V_0 = -V_{CC}RC_0f,$$

where $f$ is the input frequency. Adjust the 10-kΩ potentiometer to calibrate the converter.

The 1- and 0.1-μF capacitors smooth the transients that result from the rapid switching. For the figure’s values, the output ranges from 0 to −10V for inputs of 0 to 10 kHz. If you need higher-frequency operation, you must consider the effects of rapid switching on the CMOS inverter’s supply current. Because a CMOS IC’s power dissipation is proportional to frequency, you can simply add its supply current to the capacitor’s discharge current in the calculations.

You can make a frequency summer by exploiting the fact that there are six Schmitt triggers per package: Attach a capacitor to each inverter’s output, apply a different frequency to each input, and obtain $V_0$ proportional to the sum of the input frequencies:

$$V_0 = -V_{CC}R(C_1f_1 + C_2f_2 + \ldots + C_6f_6).$$

Moreover, you can extend the technique by paralleling additional ICs.

With the figure’s component values, the F/V converter yields ±0.4% max nonlinearity for inputs of 0 to 10 kHz.

Figure 1 Using a capacitively loaded IC’s supply-current/frequency dependence, this F/V converter yields 0 to −10V output with 0- to 10-kHz input frequencies. By paralleling more Schmitt triggers, you can use the circuit as a frequency summer.