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Clock Generation

WEB-CONFIGURABLE FACTORY-CUSTOMIZED CLOCK GENERATORS AVAILABLE AT: www.silabs.com/custom-timing

Differential + LVCMOS Clocks
Silicon Labs’ differential + LVCMOS clock generators provide any rate, any output frequency synthesis. Any combination of output frequencies can be generated exactly with 0 ppm error. Independent signal format and VDDO options provide integrated level translation, supporting LVPECL/LVDS/HCSL/LVCMOS clock generation up to 710 MHz with sub 1 ps rms phase jitter. Low jitter, low power PCI Express clocks with a wide variety of output options are also available.

Si5338 FEATURES
- Generates any frequency on any output, from 160 kHz to 350 MHz and select frequencies to 710 MHz
- Exact clock synthesis (0 ppm error)
- Crystal or clock input
- 4 differential outputs or 8 single-ended outputs
- Any format, on any output: LVPECL, LVDS, HCSL, LVCMOS, HSTL, SSTL and CML
- Independent VDDO per output eliminates external level translators (1.5, 1.8, 2.5, 3.3 V)
- Low phase jitter: 1 ps rms
- I²C programmable or pin-controlled
- Excellent PSRR, no discrete components
- Spread spectrum clock generation
- Spread modulation frequency: 16 to 128 kHz
- Spread percentage: 0.1 to 5%
- User-definable control pins: Powerdown, Output Enable, Frequency Select, Spread Select
- Programmable tr/τf options

DATACOM LINE CARD

PART NUMBER | CONTROL | CLOCK INPUT/OUTPUTS | INPUT FREQUENCY (MHz) | OUTPUT FREQUENCY (MHz) | PHASE JITTER (RMS) | VDD | VDDO | OUTPUT | PACKAGE |
--- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
Si5334 | Pin | 1/4 | 5 - 710 (Clock), 8 - 30 (Xtal) | 0.16 - 710 MHz 0.16 - 350 MHz 0.16 - 200 MHz | 1.0 ps | 1.8, 2.5, 3.3 V | 1.8, 2.5, 3.3 V | LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL | QFN24 |
Si5335 | Pin | 1/4 | 10 - 350 (Clock), 25/27 (Xtal) | 1 - 350 MHz | 1.0 ps | 1.8, 2.5, 3.3 V | 1.8, 2.5, 3.3 V | LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL | QFN24 |
Si5338 | I2C | 1/4 | 5 - 710 (Clock), 8 - 30 (Xtal) | 0.16 - 710 MHz 0.16 - 350 MHz 0.16 - 200 MHz | 1.0 ps | 1.8, 2.5, 3.3 V | 1.8, 2.5, 3.3 V | LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML | QFN24 |
LVCMOS Clocks (1-4 Outputs)

Silicon Labs’ highly flexible, factory and I²C programmable tiny clock LVCMOS generators can be customized to generate multiple frequencies with significantly lower jitter, lower power and smaller size than competing solutions. Customization options are available to minimize EMI, including customizable spread percentage, modulation rate, output impedance and rise time/fall time.

**Si512xx Tiny Clock Features**
- Up to three customizable output frequencies from 3 to 200 MHz
- Accepts 8 to 48 MHz crystal or 3 to 166 MHz external reference clock
- Low cycle-to-cycle jitter: <150 ps
- Low power: 2.3 mA (typ) at 48 MHz output, 25 MHz xtal in and VDD = 3.3 V
- Center spread modulation from 0.25 to 1.0%, with 0.125% resolution
- Programmable spread modulation rate from 30 - 62 kHz
- Customizable drive strengths (four levels for each output)
- Customizable control pins (PD#/OE/SSON#/FS)
- Supply range: 1.8 V for Si51214; 2.5 to 3.3 V for other devices
- Ultra-compact packages
  - 6-pin TDFN (1.2 mm x 1.4 mm x 0.75 mm)
  - 8-pin TDFN (1.6 mm x 1.4 mm x 0.75 mm)
- Factory programmable OTP
- Two week sample lead time
LVCMOS Clocks (5+ Outputs)

Silicon Labs’ highly flexible factory and I2C programmable LVCMOS clock generators can be customized to generate multiple independent non-integer-related frequencies with equivalent frequency synthesis capability of 8 PLLs, with exact frequency synthesis (0 ppm error) significantly lower jitter, lower power and smaller size than competing solutions. Factory customization options are available to minimize EMI, including configurable edge rates, output impedance, output skew and spread spectrum.

**Si5350 FEATURES**

- Generates any frequency on any output, 8 kHz to 160 MHz
- Exact clock synthesis: 0 ppm error
- Similar frequency flexibility as 8 independent PLLs
- Crystal or clock input
- <100 ps pk-pk period jitter
- Glitchless switching between output frequencies
- I2C programmable or pin-controlled

- Excellent PSRR: no discrete components
- Two week sample lead time for any custom clock
- Integrated load capacitors
- Spread spectrum clock generation
  - 0.5 to -2.5% down, ±0.1 to ±1.5% center
- User-definable control pins Powerdown, Output Enable, Spread Enable, Frequency Select control pins

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CONTROL</th>
<th>CLOCK INPUT/OUTPUTS</th>
<th>INPUT FREQUENCY [MHz]</th>
<th>OUTPUT FREQUENCY [MHz]</th>
<th>PERIOD JITTER [PP]</th>
<th>VDD</th>
<th>VDDO</th>
<th>OUTPUT</th>
<th>PACKAGE</th>
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<td>Si5350A/51A</td>
<td>Pin/I2C</td>
<td>1/8</td>
<td>25/27 (Xtal)</td>
<td>8 kHz - 160 MHz</td>
<td>100 ps</td>
<td>2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVCMOS</td>
<td>QFN20/QSOP24</td>
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<td>Si5350B/51B</td>
<td>Pin/I2C</td>
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<td>25/27 (Xtal)</td>
<td>8 kHz - 160 MHz</td>
<td>100 ps</td>
<td>2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVCMOS</td>
<td>QFN20/QSOP24</td>
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<td>Pin/I2C</td>
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<td>10 - 100 (Clock), 25/27 (Xtal)</td>
<td>8 kHz - 160 MHz</td>
<td>100 ps</td>
<td>2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVCMOS</td>
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<td>50 ps</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
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<td>QFN24</td>
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<td>SL38160</td>
<td>Pin/I2C</td>
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<td>3 - 166 (Clock), 8 - 48 (Xtal)</td>
<td>3 - 200 MHz</td>
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<td>1.8, 2.5, 3.3 V</td>
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PCI Express (PCIe) Gen 1/2/3 Clocks and Buffers

Silicon Labs has the lowest jitter clocks and buffers for PCIe Gen 1/2/3. To optimize performance, the devices support programmable drive strength, rise/fall times and output impedance. Basic HCSL PCIe and high-performance differential clocks and buffers are available. Support for down and center spread spectrum clock generation is also provided.

PCIe CLOCK AND BUFFER FEATURES

- Full portfolio of PCI Express (PCIe) Gen 1/2/3 clocks and buffers
- Range of available external ref clock or crystal input frequencies
- Fully integrated termination resistors on PCIe outputs
- Low power consumption
- Programmable spread spectrum
- Available hardware strapping pin for spread enable
- I2C/SMBus programmable
- Externally convertible outputs to LVDS or LVPECL
- Support industrial temperature grade

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CONTROL</th>
<th>CLOCK INPUT/OUTPUTS</th>
<th>INPUT FREQUENCY (MHz)</th>
<th>OUTPUT FREQUENCY (MHz)</th>
<th>PHASE JITTER (RMS)</th>
<th>VDD VDDO</th>
<th>OUTPUT</th>
<th>PACKAGE</th>
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<td>100 MHz, 25 MHz</td>
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<td>3.3 V</td>
<td>3.3 V</td>
<td>HSCL, LVC MOS</td>
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<td>3.3 V</td>
<td>HSCL</td>
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<td>HSCL</td>
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<td>HSCL</td>
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<td>Pin/IC</td>
<td>2/4</td>
<td>25 MHz/100 MHz</td>
<td>100 MHz</td>
<td>1.0 ps</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>HSCL</td>
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<td>1.0 ps</td>
<td>3.3 V</td>
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<td>HSCL</td>
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<td>3.3 V</td>
<td>3.3 V</td>
<td>HSCL</td>
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<td>3.3 V</td>
<td>3.3 V</td>
<td>HSCL</td>
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<td>HSCL</td>
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<td>1.0 ps</td>
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<td>3.3 V</td>
<td>HSCL</td>
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<td>1.0 ps</td>
<td>3.3 V</td>
<td>3.3 V</td>
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<td>Si53159</td>
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<td>3.3 V</td>
<td>3.3 V</td>
<td>HSCL</td>
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<td>CY8400-2</td>
<td>Pin/IC</td>
<td>1/4</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>—</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>HSCL</td>
</tr>
<tr>
<td>CY88800</td>
<td>Pin/IC</td>
<td>1/6</td>
<td>100 MHz</td>
<td>100 MHz</td>
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<td>3.3 V</td>
<td>3.3 V</td>
<td>HSCL</td>
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<tr>
<td>Si5334</td>
<td>Pin</td>
<td>1/4</td>
<td>5 - 710 (Clock), 8 - 30 (Xtal)</td>
<td>0.16 - 710 MHz</td>
<td>1.0 ps</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVC MOS, LVDS, LVPECL, HCSL, SSTL, HSTL</td>
</tr>
<tr>
<td>Si5335</td>
<td>Pin</td>
<td>1/4</td>
<td>10 - 350 (Clock), 25 - 27 (Xtal)</td>
<td>1 - 350 MHz</td>
<td>1.0 ps</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVC MOS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML</td>
</tr>
<tr>
<td>Si5338</td>
<td>Pin</td>
<td>1/4</td>
<td>5 - 710 (Clock), 8 - 30 (Xtal)</td>
<td>0.16 - 710 MHz</td>
<td>1.0 ps</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVPECL, LVDS, LVC MOS, HCSL, SSTL, HSTL</td>
</tr>
</tbody>
</table>
Integrated Clock + VCXO Solutions

These integrated clock + VCXO devices feature an integrated voltage controlled oscillator (VCXO), while eliminating the need for custom, pullable crystals. Free-running and VCXO clocks can be generated by one device, making them ideal for cost-sensitive consumer applications.

Si5350B/51B FEATURES

- Generates any frequency on any output, 8 kHz to 160 MHz
- Exact clock synthesis: 0 ppm error
- Similar frequency flexibility as 8 independent PLLs
- Accepts crystal and analog control voltage input (VCXO)
- <100 ps pk-pk period jitter for any configuration
- Glitchless switching between output frequencies
- Integrated VCXO uses standard non-pullable crystal
- I2C programmable or pin-controlled
- Excellent PSRR: no discrete components
- Two week sample lead time for any custom clock
- Integrated load capacitors
- Spread spectrum clock generation -0.5 to -2.5% down, ±0.1 to ±1.5% center
- User-definable control pins Powerdown, Output Enable, Spread Enable or Frequency Select control pins
Embedded Intel x86 Clocks

Silicon Labs offers an extensive family of Intel-compliant x86 clocks for embedded computing, communications and industrial applications. These system main clock generators support a wide variety of chipsets and processors. They provide all the necessary clock generation for the CPU, memory controller (chipset north bridge), I/O controller (chipset south bridge) as well as the latest timing requirements for industry standards such as SATA, USB, LAN, PCI Express, and legacy PCI.

**EMBEDDED INTEL x86 CLOCK FEATURES**

- Clocking support for Intel processors
- Multi-PLL platform for independent, asynchronous signal generation
- Low power consumption push-pull differential buffers
- Available true differential current steering buffers
- Signal power management for notebook applications
- Dynamic enable/disable for PCIe hot plug applications
- Integrated voltage regulator and damping resistors on differential clocks
- Integrates external graphics clocking requirements
- Available center spread LCD clock for optimized display screen EMI reduction
- Integrated LAN clock for cost/space/component savings
- Integrated IEEE1394 clock for cost/space component savings
- 8-step programmable slew rate control for rise time and fall time control
- Dynamic independent PLL overclocking for enthusiast applications
- Underclocking capabilities for power management support and debugging
- Best in the industry pread pectrum technology for optimum system EMI reduction

**EMBEDDED PC**

- SL28EB717 Embedded Intel x86 Clock
- CPU
- PCIe x 1
- PCIe x 1
- PCIe
- LPC
- 3 PCIe x 1
- SD/MMC
- USB 2.0
- Ethernet
- PCIe
- PCIe
- DDR II
- SDVO
- LVDS
- BIOS
- HCSL
- 5
- PCIe
- MBR/100 MHz
- DOT 96, 96 MHz
- SATA75, 75 MHz
- USB-48, 48 MHz
- SYSCLK-25, 25 MHz
- PCI, 33.3 MHz
- PCI Devices
## Embedded Intel x86 Clocks [cont.]

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CONTROL</th>
<th>CLOCK INPUT/OUTPUTS</th>
<th>INPUT FREQUENCY (MHz)</th>
<th>OUTPUT FREQUENCY (MHz)</th>
<th>VDD</th>
<th>VDDO</th>
<th>OUTPUT</th>
<th>PACKAGE</th>
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<tbody>
<tr>
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<td>Pin/°C</td>
<td>1/20</td>
<td>14.318 MHz</td>
<td>14.3 MHz, 33 MHz, 48 MHz, 96 MHz, 100 MHz, 100 MHz-200 MHz</td>
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<td>3.3 V</td>
<td>LVCOS, HCSL</td>
<td>TSSOP56</td>
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<td>Pin/°C</td>
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<td>14.318 MHz</td>
<td>14.3 MHz, 24.576 MHz, 25 MHz, 33 MHz, 48 MHz, 96 MHz, 100 MHz, 100 MHz-167 MHz, 100 MHz-400.65 MHz</td>
<td>3.3 V</td>
<td>3.3 V - 1.05 V</td>
<td>LVCOS</td>
<td>TSSOP64</td>
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<td>CY28551</td>
<td>Pin/°C</td>
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<td>CY99530</td>
<td>Pin/°C</td>
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<td>25 - 33 MHz</td>
<td>25 MHz-133 MHz</td>
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<td>LVCOS</td>
<td>SSOP48/TSSOP48</td>
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<td>CY99531</td>
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<td>TSSOP64</td>
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<td>TSSOP64</td>
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<td>3.3 V - 1.05 V</td>
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<td>3.3 V - 1.05 V</td>
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<td>QFN48</td>
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<td>14.318 MHz</td>
<td>14.318 MHz, 27 MHz, 96 MHz, 100 MHz, 133 MHz, 166 MHz, 200 MHz, 266 MHz, 333 MHz, 400 MHz</td>
<td>3.3 V</td>
<td>3.3 V - 1.05 V</td>
<td>LVCOS, HCSL</td>
<td>QFN32</td>
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<tr>
<td>SL28EB717</td>
<td>Pin/°C</td>
<td>1/13</td>
<td>25 MHz</td>
<td>12 MHz, 14.318 MHz, 25 MHz, 27 MHz, 33 MHz, 48 MHz, 96 MHz, 100 MHz, 133 MHz, 166 MHz, 200 MHz, 266 MHz, 333 MHz, 400 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>LVCOS, HCSL</td>
<td>48QFN</td>
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<tr>
<td>SL28EB719</td>
<td>Pin/°C</td>
<td>1/13</td>
<td>25 MHz</td>
<td>12 MHz, 14.318 MHz, 25 MHz, 27 MHz, 33 MHz, 48 MHz, 96 MHz, 100 MHz, 133 MHz, 166 MHz, 200 MHz, 266 MHz, 333 MHz, 400 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>LVCOS, HCSL</td>
<td>TSSOP48</td>
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<tr>
<td>SL28EB740</td>
<td>Pin/°C</td>
<td>1/16</td>
<td>25 MHz</td>
<td>12 MHz, 14.318 MHz, 25 MHz, 27 MHz, 33 MHz, 48 MHz, 96 MHz, 100 MHz, 133 MHz, 166 MHz, 200 MHz, 266 MHz, 333 MHz, 400 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>LVCOS, HCSL</td>
<td>TSSOP64</td>
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<tr>
<td>SL28EB742</td>
<td>Pin/°C</td>
<td>1/16</td>
<td>14.318 MHz</td>
<td>14.3 MHz, 33 MHz, 48 MHz, 96 MHz, 100 MHz, 133 MHz, 166 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>LVCOS, HCSL</td>
<td>QFN56</td>
</tr>
</tbody>
</table>
EMI Reduction Clocks

Silicon Labs’ programmable spread spectrum clock generators feature a wide range of programming options allowing system designers to minimize EMI at the application level. Configurable parameters include spread spectrum percentage/modulation rate, programmable edge rates, programmable output impedance and programmable skew.

EMI REDUCTION CLOCK FEATURES

- Output frequencies from 1 to 200 MHz
- CLKOUT, REFCLK or SSCLK output options
- CLKIN or XO input options
- 8 to 48 MHz crystal input range
- 1 to 166 MHz clock input range
- Spread percent from 0 to 5.0%
- Down or center spread options
- Spread modulation frequency from 16 to 128 kHz
- On-chip programmable crystal capacitive load (C< sub >L< /sub >): 8 to 20 pF
- User-definable control pins Powerdown, Output Enable, Spread Enable, Frequency Select, Spread Select control pins
- 7 programmable tr/ff options
- Smallest SSCG clock on the market (TDFN6 1.2 x 1.4 mm)

---

**PART NUMBER | CONTROL | CLOCK INPUT/OUTPUTS | INPUT FREQUENCY [MHz] | OUTPUT FREQUENCY [MHz] | PHASE JITTER [pps] | VDD | VDDO | OUTPUT | PACKAGE**
--- | --- | --- | --- | --- | --- | --- | --- | --- | ---
SL15300 | Pin | 1/4 | 3 - 166 (Clock), 8 - 48 (Xtal) | 3 - 200 MHz | — | 1.8, 2.5, 3.3 V | — | LVCMS | TSSOP8
SL16020DC | Pin/I2C | 1/2 | 27 (Xtal) | 27 MHz, 100 MHz | — | 3.3 V | — | LVCMS | TDFN10
Si5335 | Pin | 1/4 | 10 - 350 (Clock), 25/27 (Xtal) | 1 - 350 MHz | 1.0 ps | 1.8, 2.5, 3.3 V | 1.8, 2.5, 3.3 V | LVCMS, LVDS, LVPECL, HCSL, SSTL, HSTL, CML | QFN24
Si51210 | Pin | 1/2 | 3 - 166 (Clock), 8 - 48 (Xtal) | 3 - 200 MHz | — | 2.5 - 3.3 V | — | LVCMS | TDFN6
Si51211 | Pin | 2/3 | 3 - 166 (Clock), 8 - 48 (Xtal) | 3 - 200 MHz | — | 2.5 - 3.3 V | 1.8, 2.5, 3.3 V | LVCMS | TDFN6
Si51214 | Pin | 1/2 | 3 - 166 (Clock), 8 - 48 (Xtal) | 3 - 200 MHz | — | 1.8 V | — | LVCMS | TDFN6
Si51219 | Pin | 2/3 | 3 - 166 (Clock), 8 - 48 (Xtal) | 3 - 200 MHz | — | 2.5 - 3.3 V | 1.8, 2.5, 3.3 V | LVCMS | TSSOP8
Si51242 | Pin/I2C | 1/3 | 25 MHz | 100 MHz, 25 MHz | 1.0 ps | 3.3 V | 3.3 V | HSCL, LVCMS | QFN24
Si51243 | Pin/I2C | 1/5 | 25 MHz | 100 MHz, 25 MHz | 1.0 ps | 3.3 V | 3.3 V | HSCL, LVCMS | QFN24
Si51244 | Pin/I2C | 1/4 | 25 MHz | 100 MHz | 1.0 ps | 3.3 V | 3.3 V | HSCL | QFN24
Si51246 | Pin/I2C | 1/6 | 25 MHz | 100 MHz | 1.0 ps | 3.3 V | 3.3 V | HSCL | QFN32
Si51247 | Pin/I2C | 1/9 | 25 MHz | 100 MHz | 1.0 ps | 3.3 V | 3.3 V | HSCL | QFN48
Clock Buffers

WEB-CONFIGURABLE CUSTOM CLOCK BUFFERS AVAILABLE AT: www.silabs.com/ClockBuilder

Fanout Buffers (non-PLL)

Silicon Labs’ low jitter clock buffers produce multiple copies of an input clock at the same frequency with minimal additive jitter. LVDS, LVPECL, HCSL, CML, LVCMOS, SSTL and HSTL buffers are available, including devices that support multiple formats per device.

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CONTROL</th>
<th>CLOCK INPUT/OUTPUTS</th>
<th>ADDITIVE JITTER (RMS)</th>
<th>INPUT FREQUENCY (MHz)</th>
<th>OUTPUT FREQUENCY (MHz)</th>
<th>VDD</th>
<th>VDDO</th>
<th>OUTPUT</th>
<th>PACKAGE</th>
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<tbody>
<tr>
<td>Si53302</td>
<td>Pin</td>
<td>2/10</td>
<td>100 fs</td>
<td>1 - 725 MHz</td>
<td>1 - 725 MHz</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5 V</td>
<td>LVCMOS, LVDS, LVPECL, HCSL, CML</td>
<td>QFN44</td>
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<tr>
<td>Si53303</td>
<td>Pin</td>
<td>2/10</td>
<td>100 fs</td>
<td>1 - 725 MHz</td>
<td>1 - 725 MHz</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5 V</td>
<td>LVCMOS, LVDS, LVPECL, HCSL, CML</td>
<td>QFN44</td>
</tr>
<tr>
<td>Si53315</td>
<td>Pin</td>
<td>2/10</td>
<td>100 fs</td>
<td>1 - 1250 MHz</td>
<td>1 - 1250 MHz</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5 V</td>
<td>LVCMOS, LVDS, LVPECL, HCSL, CML</td>
<td>QFN44</td>
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<tr>
<td>Si53320</td>
<td>Pin</td>
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<td>100 fs</td>
<td>1 - 725 MHz</td>
<td>1 - 725 MHz</td>
<td>2.5, 3.3 V</td>
<td>2.5, 3.3 V</td>
<td>LVPECL</td>
<td>TSSOP20</td>
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<tr>
<td>Si53360</td>
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<td>100 fs</td>
<td>1 - 200 MHz</td>
<td>1 - 200 MHz</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5 V</td>
<td>LVCMOS</td>
<td>TSSOP16</td>
</tr>
<tr>
<td>Si53152</td>
<td>Pin/I2C</td>
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<td>1.0 ps</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>HCSL</td>
<td>QFN24</td>
</tr>
<tr>
<td>Si53154</td>
<td>Pin/I2C</td>
<td>1/4</td>
<td>1.0 ps</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>HCSL</td>
<td>QFN24</td>
</tr>
<tr>
<td>Si53156</td>
<td>Pin/I2C</td>
<td>1/6</td>
<td>1.0 ps</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>HCSL</td>
<td>QFN32</td>
</tr>
<tr>
<td>Si53159</td>
<td>Pin/I2C</td>
<td>1/9</td>
<td>1.0 ps</td>
<td>100 MHz</td>
<td>100 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>HCSL</td>
<td>QFN48</td>
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<tr>
<td>SL235NZ</td>
<td>Pin</td>
<td>1/4</td>
<td>—</td>
<td>1 - 140 MHz</td>
<td>1 - 140 MHz</td>
<td>3.3 V</td>
<td>—</td>
<td>LVCMOS</td>
<td>STSOP18SDIC</td>
</tr>
<tr>
<td>SL23EP04NZ</td>
<td>Pin</td>
<td>1/4</td>
<td>—</td>
<td>DC - 220 MHz</td>
<td>DC - 220 MHz</td>
<td>2.5 V, 3.3 V</td>
<td>—</td>
<td>LVCMOS</td>
<td>TSSOP8</td>
</tr>
<tr>
<td>SL2305NZ</td>
<td>Pin</td>
<td>1/5</td>
<td>—</td>
<td>1 - 140 MHz</td>
<td>1 - 140 MHz</td>
<td>3.3 V</td>
<td>—</td>
<td>LVCMOS</td>
<td>STSOP8/SOIC8</td>
</tr>
<tr>
<td>SL2309NZ</td>
<td>Pin</td>
<td>1/9</td>
<td>—</td>
<td>DC - 140 MHz</td>
<td>DC - 140 MHz</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>LVCMOS</td>
<td>SOIC16</td>
</tr>
<tr>
<td>SL23EP09NZ</td>
<td>Pin</td>
<td>1/9</td>
<td>—</td>
<td>DC - 140 MHz</td>
<td>DC - 140 MHz</td>
<td>2.5 V, 3.3 V</td>
<td>—</td>
<td>LVCMOS</td>
<td>STSOP16/SOIC16</td>
</tr>
<tr>
<td>SL28PCle14</td>
<td>Pin/I2C</td>
<td>2/4</td>
<td>1.0 ps</td>
<td>25 MHz/100 MHz</td>
<td>100 MHz</td>
<td>3.3 V</td>
<td>—</td>
<td>HCSL</td>
<td>QFN32</td>
</tr>
<tr>
<td>Si5310</td>
<td>Pin</td>
<td>1/4</td>
<td>150 fs</td>
<td>5 - 710 MHz</td>
<td>5 - 710 MHz</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVPECL, LVDS, HCSL, SSTL, HSTL</td>
<td>QFN24</td>
</tr>
<tr>
<td>Si5330F</td>
<td>Pin</td>
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<td>—</td>
<td>5 - 200 MHz</td>
<td>5 - 200 MHz</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVCMOS</td>
<td>QFN24</td>
</tr>
<tr>
<td>Si5335</td>
<td>Pin</td>
<td>1/4</td>
<td>150 fs</td>
<td>1 - 350 MHz</td>
<td>1 - 350 MHz</td>
<td>1.8, 2.5, 3.3 V</td>
<td>1.8, 2.5, 3.3 V</td>
<td>LVCMOS, LVDS, LVPECL, HCSL, SSTL, HSTL</td>
<td>QFN24</td>
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<tr>
<td>SL18860DC</td>
<td>Pin</td>
<td>1/3</td>
<td>—</td>
<td>10 - 52 MHz</td>
<td>10 - 52 MHz</td>
<td>1.8, 2.5, 3.3 V</td>
<td>—</td>
<td>LVCMOS</td>
<td>TDFN10</td>
</tr>
</tbody>
</table>

- Non-PLL based clock distribution
- 1:10 LVPECL, LVDS, HCSL, CML buffers
- 1:20 CMOS/SSTL/HSTL buffers
- 2:1 input mux with glitchless input clock switch
- Synchronous output enable
- Low jitter: as low as 100fs typ (12 kHz – 20 MHz)
- Wide operation frequency from DC to 1.25 GHz
- Integrated level translation
- Low propagation delay
- Low output-to-output skew
- Low device-to-device skew
- Multiple drive strength options
- Wide operation frequency from DC to 1.25 GHz
- 1.8, 2.5, 3.3 V operation
- Multiple formats per device
Zero Delay Buffers (PLL)

Silicon Labs’ zero delay clock buffers are used in applications that require zero propagation delay between the input and output clocks. Silicon Labs’ zero delay buffers provide low power consumption and simplify the distribution of spread spectrum clocks.

**ZERO DELAY BUFFER FEATURES**

- Low propagation delay
- Low output-to-output skew
- Low device-to-device skew
- Low output jitter
- Drive strength options
- Wide operation frequency from 10 to 220 MHz
- 3.3 V to 2.5 V power supply range
- Low power dissipation

---

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CONTROL</th>
<th>CLOCK INPUT/OUTPUTS</th>
<th>INPUT FREQUENCY (MHz)</th>
<th>OUTPUT FREQUENCY (MHz)</th>
<th>PHASE JITTER (RMS)</th>
<th>VDD</th>
<th>VDD0</th>
<th>OUTPUT</th>
<th>PACKAGE</th>
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<tbody>
<tr>
<td>SL2305</td>
<td>Pin</td>
<td>1/5</td>
<td>1 - 140 MHz</td>
<td>1 - 140 MHz</td>
<td>—</td>
<td>3.3 V</td>
<td>—</td>
<td>LVCMS</td>
<td>TSSOP8/SOIC8</td>
</tr>
<tr>
<td>SL2309</td>
<td>Pin</td>
<td>1/9</td>
<td>10 - 140 MHz</td>
<td>10 - 140 MHz</td>
<td>—</td>
<td>3.3 V</td>
<td>—</td>
<td>LVCMS</td>
<td>TSSOP16/SOIC16</td>
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<td>SL23EP04</td>
<td>Pin</td>
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<td>10 - 220 MHz</td>
<td>10 - 220 MHz</td>
<td>—</td>
<td>2.5 V, 3.3 V</td>
<td>—</td>
<td>LVCMS</td>
<td>SOIC8</td>
</tr>
<tr>
<td>SL23EP05</td>
<td>Pin</td>
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<td>10 - 220 MHz</td>
<td>10 - 220 MHz</td>
<td>—</td>
<td>2.5 V, 3.3 V</td>
<td>—</td>
<td>LVCMS</td>
<td>TSSOP8/SOIC8</td>
</tr>
<tr>
<td>SL23EP08</td>
<td>Pin</td>
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<td>10 - 220 MHz</td>
<td>10 - 220 MHz</td>
<td>—</td>
<td>2.5 V, 3.3 V</td>
<td>—</td>
<td>LVCMS</td>
<td>TSSOP16/SOIC16</td>
</tr>
<tr>
<td>SL23EP09</td>
<td>Pin</td>
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<td>10 - 220 MHz</td>
<td>10 - 220 MHz</td>
<td>—</td>
<td>2.5 V, 3.3 V</td>
<td>—</td>
<td>LVCMS</td>
<td>TSSOP16/SOIC16</td>
</tr>
</tbody>
</table>
Silicon Labs’ precision clocks generate any output frequency from any input frequency while providing jitter attenuation and clock distribution in high-performance timing applications requiring sub 0.5 ps jitter performance. The devices accept multiple clock inputs ranging from 2 kHz to 710 MHz and generate multiple low jitter, independent, synchronous clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The precision clocks are based on Silicon Labs’ proven third-generation DSPLL® technology, which generates any output frequency from any input frequency with 300 fs rms jitter performance in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components.

**JITTER ATTENUATOR FEATURES**
- Generates any output frequency from any input frequency
- Ultra-low jitter: 290 fs RMS
- 1-DSPLL and 4-DSPLL versions available
- Integrated loop filter with selectable loop bandwidth
- Hitless switching with phase buildout (auto/manual)
- Freerun or synchronous operating modes
- Best-in-class PSRR
- I2C/SPI or pin-controlled
- User-selectable output clock signal format (LVPECL, LVDS, CML, CMOS)
- Single supply: 1.8, 2.5 or 3.3 V ±10% operation
- Easy-to-use DSPLLsim® configuration software

*see page 16 for more about our DSPLLsim software*
Silicon Labs’ crystal oscillators and voltage controlled crystal oscillators (XO/VCXOs) leverage advanced DSPLL® circuitry to provide a low jitter clock at any frequency from 100 kHz to 1.4 GHz. Unlike a traditional XO, where a different crystal is required for each output frequency, Silicon Labs’ XO/VCXOs use one fixed frequency crystal to provide a wide range of output frequencies. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability, while providing best-in-class jitter performance and supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments. All devices are factory configurable for a wide variety of user specifications including frequency, supply voltage, output format and stability, thereby eliminating long lead times associated with custom oscillators.

XOs/VCXOs

REQUEST CUSTOM PART NUMBERS AND SAMPLES AT: www.silabs.com/VCXOpartnumber

Fixed Frequency XO/VCXOs

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TYPE</th>
<th>FREQUENCY</th>
<th>FREQUENCY RANGE</th>
<th>RMS PHASE JITTER</th>
<th>STABILITY/APR (PPM)</th>
<th>OUTPUT FORMAT</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si510/1</td>
<td>XO</td>
<td>Single</td>
<td>0.1 - 250 MHz</td>
<td>0.8 ps</td>
<td>±30, ±50, ±100</td>
<td>LVPECL, LVDS, HCSL, Dual CMOS, LVCMOS,</td>
<td>5 mm x 7 mm and 3.2 mm x 5 mm 6-pad</td>
</tr>
<tr>
<td>Si512/3</td>
<td>XO</td>
<td>Dual</td>
<td>0.1 - 250 MHz</td>
<td>0.8 ps</td>
<td>±30 to ±100</td>
<td>LVPECL, LVDS</td>
<td>5 x 7 mm 6-pad</td>
</tr>
<tr>
<td>Si515</td>
<td>VCXO</td>
<td>Single</td>
<td>0.1 - 250 MHz</td>
<td>1.0 ps</td>
<td>±30 to ±100</td>
<td>LVPECL, LVDS</td>
<td>5 x 7 mm 6-pad</td>
</tr>
<tr>
<td>Si516</td>
<td>VCXO</td>
<td>Dual</td>
<td>0.1 - 250 MHz</td>
<td>1.0 ps</td>
<td>±30 to ±100</td>
<td>LVPECL, LVDS</td>
<td>5 x 7 mm 6-pad</td>
</tr>
<tr>
<td>Si530/1</td>
<td>XO</td>
<td>Single</td>
<td>10 - 1417 MHz</td>
<td>0.3 ps</td>
<td>±20, ±31.5, ±61.5</td>
<td>LVPECL, LVDS</td>
<td>5 x 7 mm 6-pad</td>
</tr>
<tr>
<td>Si532/3</td>
<td>XO</td>
<td>Dual</td>
<td>10 - 1417 MHz</td>
<td>0.3 ps</td>
<td>±20, ±31.5, ±61.5</td>
<td>LVPECL, LVDS</td>
<td>5 x 7 mm 6-pad</td>
</tr>
<tr>
<td>Si534</td>
<td>XO</td>
<td>Quad</td>
<td>10 - 1417 MHz</td>
<td>0.3 ps</td>
<td>±20, ±31.5, ±61.5</td>
<td>LVPECL, LVDS</td>
<td>5 x 7 mm 6-pad</td>
</tr>
<tr>
<td>Si536/6</td>
<td>XO</td>
<td>Quad</td>
<td>100 - 312.5 MHz</td>
<td>0.19 ps rms</td>
<td>±20, ±31.5</td>
<td>LVPECL, LVDS</td>
<td>5 x 7 mm 6-pad</td>
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<tr>
<td>Si550</td>
<td>VCXO</td>
<td>Single</td>
<td>10 - 1417 MHz</td>
<td>0.5 ps</td>
<td>±12 to ±375</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>5 x 7 mm 6-pad</td>
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<tr>
<td>Si552</td>
<td>VCXO</td>
<td>Dual</td>
<td>10 - 1417 MHz</td>
<td>0.5 ps</td>
<td>±12 to ±375</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>5 x 7 mm 6-pad</td>
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<tr>
<td>Si554</td>
<td>VCXO</td>
<td>Quad</td>
<td>10 - 1417 MHz</td>
<td>0.5 ps</td>
<td>±12 to ±375</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>5 x 7 mm 6-pad</td>
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<tr>
<td>Si555</td>
<td>VCXO</td>
<td>Single</td>
<td>100 - 312.5 MHz</td>
<td>0.5 ps</td>
<td>±10 to ±370</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>5 x 7 mm 6-pad</td>
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<tr>
<td>Si556</td>
<td>VCXO</td>
<td>Quad</td>
<td>100 - 312.5 MHz</td>
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<td>±10 to ±370</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>5 x 7 mm 6-pad</td>
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</table>

I2C Programmable XO/VCXOs

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TYPE</th>
<th>FREQUENCY RANGE</th>
<th>TUNING RESOLUTION</th>
<th>RMS PHASE JITTER</th>
<th>STABILITY/APR (PPM)</th>
<th>OUTPUT FORMAT</th>
<th>SUPPLY VOLTAGE (V)</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si514</td>
<td>XO</td>
<td>0.1 - 250 MHz</td>
<td>26 PPT</td>
<td>0.8 ps</td>
<td>±30, ±50, ±100</td>
<td>HCSL, LVPECL, LVDS, LVCMOS, Dual CMOS,</td>
<td>1.8, 2.5, 3.3 V</td>
<td>5 x 7 mm/ 3.2 x 5 mm 6-pad</td>
</tr>
<tr>
<td>Si570</td>
<td>XO</td>
<td>10 - 1417 MHz</td>
<td>80 PPT</td>
<td>0.3 ps</td>
<td>±20, ±31.5, ±62.5</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>1.8, 2.5, 3.3 V</td>
<td>5 x 7 mm 8-pad</td>
</tr>
<tr>
<td>Si571</td>
<td>VCXO</td>
<td>10 - 1417 MHz</td>
<td>80 PPT</td>
<td>0.5 ps</td>
<td>±12 to ±375</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>1.8, 2.5, 3.3 V</td>
<td>5 x 7 mm 8-pad</td>
</tr>
<tr>
<td>Si598</td>
<td>XO</td>
<td>10 - 810 MHz</td>
<td>28 PPT</td>
<td>0.5 ps</td>
<td>±30, ±50, ±100</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>1.8, 2.5, 3.3 V</td>
<td>5 x 7 mm 8-pad</td>
</tr>
<tr>
<td>Si599</td>
<td>VCXO</td>
<td>10 - 810 MHz</td>
<td>28 PPT</td>
<td>0.7 ps</td>
<td>±10 to ±370</td>
<td>LVPECL, LVDS, CML, LVCMOS</td>
<td>1.8, 2.5, 3.3 V</td>
<td>5 x 7 mm 8-pad</td>
</tr>
</tbody>
</table>
The Si500 low cost silicon oscillator provides high reliability and excellent immunity to shock and vibration. Through the use of innovative stabilization circuitry, the need for a mechanical resonator (quartz, MEMs or SAW) is eliminated. An all-silicon solution delivers superior aging, 20 ppm temperature stability and reliable start up and operation. Given its CMOS-based architecture, the Si500 delivers significantly better failure in time (FIT) and mean time between failure (MTBF) than traditional crystal oscillators, minimizing the cost associated with field returns due to crystal quality issues. The Si500 leverages a standard CMOS IC manufacturing flow, eliminating the expensive packaging and mechanically intensive processing steps required by crystal oscillators. All devices are factory configurable for a variety of user specifications including frequency, supply voltage, and output format.

**Si500 Features**
- Quartz-free, all silicon construction
- Generates any frequency from 0.9 to 200 MHz
- Samples of any frequency available in 2 weeks
- Low jitter: 1.5 ps RMS phase jitter, 2 ps RMS period jitter
- No internal PLL
- 3.3, 2.5 and 1.8 V options
- CMOS, LVPECL, LVDS, HCSL and SSTL options
- Driver stopped, tristate, and power down options
- Footprint compatible with 3.2 mm x 5.0 mm

### Silicon Oscillators

**Request Custom Part Numbers and Samples at:** [www.silabs.com/siliconXOpartnumber](http://www.silabs.com/siliconXOpartnumber)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TYPE</th>
<th>FREQUENCY</th>
<th>TEMPERATURE STABILITY</th>
<th>TOTAL STABILITY (PPM)</th>
<th>OUTPUT FORMAT</th>
<th>FOOTPRINT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si500S</td>
<td>XO</td>
<td>0.9 - 200 MHz</td>
<td>± 20 ppm typ</td>
<td>± 150 (0-70 °C) ± 250 (0-85 °C)</td>
<td>LVCMOS, SSTL</td>
<td>3.2 x 5 mm 4-pad</td>
</tr>
<tr>
<td>Si500D</td>
<td>XO</td>
<td>0.9 - 200 MHz</td>
<td>± 20 ppm typ</td>
<td>± 150 (0-70 °C) ± 250 (0-85 °C)</td>
<td>LVPECL, LVDS, HCSL, dual output LVCMOS, diff LVCMOS, dual output SSTL, diff SSTL</td>
<td>3.2 x 5 mm 6-pad</td>
</tr>
</tbody>
</table>
Hardware and Software Support

FULL DOCUMENTATION, SOFTWARE AND APPLICATION NOTES ARE AVAILABLE AT: www.silabs.com/timing

Clock and Oscillator Development Kits

Silicon Labs offers complete tools to help designers throughout the entire development process. Both clock and oscillator solutions offer hardware and software platforms to easily set up, configure and evaluate overall device performance.

DSPLLSim Software

DSPLLSim PC-based software utility assists users with frequency planning, loop bandwidth selection and overall device configuration of Silicon Labs Jitter Attenuating Clocks. The DSPLLSim software can be used in standalone mode or can be used directly to control the Si531x/2x/6x/7x in the device evaluation kit. The DSPLLSim software provides a listing of pin/register settings based on the user-specified configuration, significantly simplifying PLL design.
**Patented Technologies**

*FIND THE TOOLS YOU NEED TO HELP WITH YOUR ENTIRE PROJECT [www.silabs.com/timing](http://www.silabs.com/timing)*

**DSPLL® Technology**

Silicon Labs invented the patented DSPLL approach to simplify the clock multiplication and jitter attenuation circuitry required in high-speed telecommunication applications. This clock technology is now the standard for replacing multiple discrete phase-locked-loop (PLL) components with a single IC that integrates digital signal processing (DSP) circuitry and an ultra-low-jitter voltage-controlled oscillator.

**MultiSynth™ Technology**

Silicon Labs’ MultiSynth technology simplifies clock generation in communication, storage and broadcast video applications. MultiSynth is a low jitter fractional divider that supports phase error correction.

Clock generators that employ this proprietary technology can produce multiple non-integer related output clocks from a single device, eliminating the need for standalone crystal oscillators and clock generator ICs. The MultiSynth approach leverages proprietary phase error cancellation circuitry to provide any-rate frequency synthesis at very low jitter of 1 ps rms typical.
Silicon Labs Makes Finding the Right Part Easy!

QUICKLY BUY OR SAMPLE PRODUCTS ON OUR WEBSITE AT www.silabs.com/custom-timing

Clock and Oscillator Design Services
Silicon Labs offers the industry’s broadest portfolio of embedded clocks and oscillators for communications, computing, broadcast video and consumer applications with the shortest lead times in the industry, with no minimum order quantities or NRE fees. Silicon Labs also provides a comprehensive clock tree design service to simplify component selection. Proposals are generated within three business days.

Parametric Search iPad App
Take the parametric search mobile! The Silicon Labs Parametric Search iPad app makes it easy to find exactly what you need for your next embedded design. Quickly jump between microcontroller, clock, oscillator, digital isolator, and isolated gate driver product families. Filter results using common technical and application requirements. Access data sheets and other documentation directly in the app and download to iBooks for offline access. Browse detailed product information – features, applications, block diagrams and even order samples and development kits, all from within the app. Offline access available—refresh data the next time you’re connected to the internet. www.silabs.com/parametric-search

Industry’s Shortest Lead Times
Low-jitter, high-performance, custom samples are available overnight, and to help you get to market faster, production quantities ship in less than 2–4 weeks. Silicon Labs’ complete portfolio of industry-leading XOs, VCXOs, clock generators, jitter attenuating clocks and clock buffers set a new standard for flexibility, performance and lead time.

Traditional Solution - 10 to 16 weeks
- Enter Order
- Quartz Blank Fab
  - Crystal Cut
  - Lapping
  - Polishing
- Blank Processing
  - Cleaning
  - X-Ray
  - Plating
- Assembly
  - Die Attach
  - Wirebond
  - Frequency Fine Tune
- Hermetic Seal & Test
  - Vacuum Bake
  - Seal
  - Final Test

Unprogrammed Stock

Enter Order

Final Programming

Silicon Labs Solution - 2 to 4 weeks
Silicon Labs’ products are designed and manufactured to ISO 9001, ISO 14001 and ISO/TS 16949 standards.